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Impurity profile measurement by harmonic analysis

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IMPURITY PROFILE MEASUREMENT BY HARMONIC ANALYSIS

by
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(date)

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Table of Contents

List of Figures

List of Figures

Abstract

This paper discusses the several procedures presently available for measuring impurity profiles in silicon wafers. A new procedure based on harmonic generation and the capacitance variation of P-N junctions is presented and the fundamental relations derived.

This procedure is tested experimentally to verify the theory and to point out its limitations and advantages encountered in actual practice. This procedure shows promise for application where speed is important.

IMPURITY PROFILE MEASUREMENT BY HARMONIC ANALYSIS

Introduction

All semiconductor electronic devices are formed from single crystals of silicon, germanium, gallium arsenide, or other semiconductor materials. The first step in fabricating silicon semiconductor devices is to slice the silicon crystal into wafers. These wafers are then "processed" through a series of steps in which the silicon surface is smoothed, extra silicon is grown epitaxially on the surface, and impurities are introduced into the crystal structure. To introduce these impurities into the crystal, the impurity, or "dopant", is selectively deposited on the surface of the wafer and then the wafer is heated to allow the impurity to diffuse into the crystal. These impurities result in n, N, N^+, π, P, or P^+ regions inside the crystal depending on the type of impurity, the crystal, the diffusion time, and the diffusion temperature. The location, width, and strength of these regions will largely determine the electrical properties of devices

fabricated on these wafers. Thus it is important to find ways to measure the impurity profile in the silicon wafers after processing in order to provide better control and understanding of silicon semiconductor devices.

Several types of doping profiles are shown in figures 1, 2, 3, 4, and 5. The log density of free electrons is plotted as a function of distance, x, from the surface of the wafer. Very high concentrations of electrons indicate a N^+ region.

Figure 1 shows a uniformly doped P type wafer with no diffusions.

Figure 2 shows the same P type wafer after an N diffusion has been driven in from the surface. Note the exponential decay of electron density as one moves away from the surface deeper into the wafer. This region is terminated by a rapid change from N type to P type. In this P-N junction region the transition from N type to P type is linear or graded.

Figure 3, in contrast to figure 2, shows an epitaxially grown N layer on a P wafer. Note that the electron density is constant throughout the N layer until the junction region is reached. This doping profile results in a step P-N junction where the transition from N type to P type is very abrupt.

Figure 4 shows an epitaxially grown N layer on

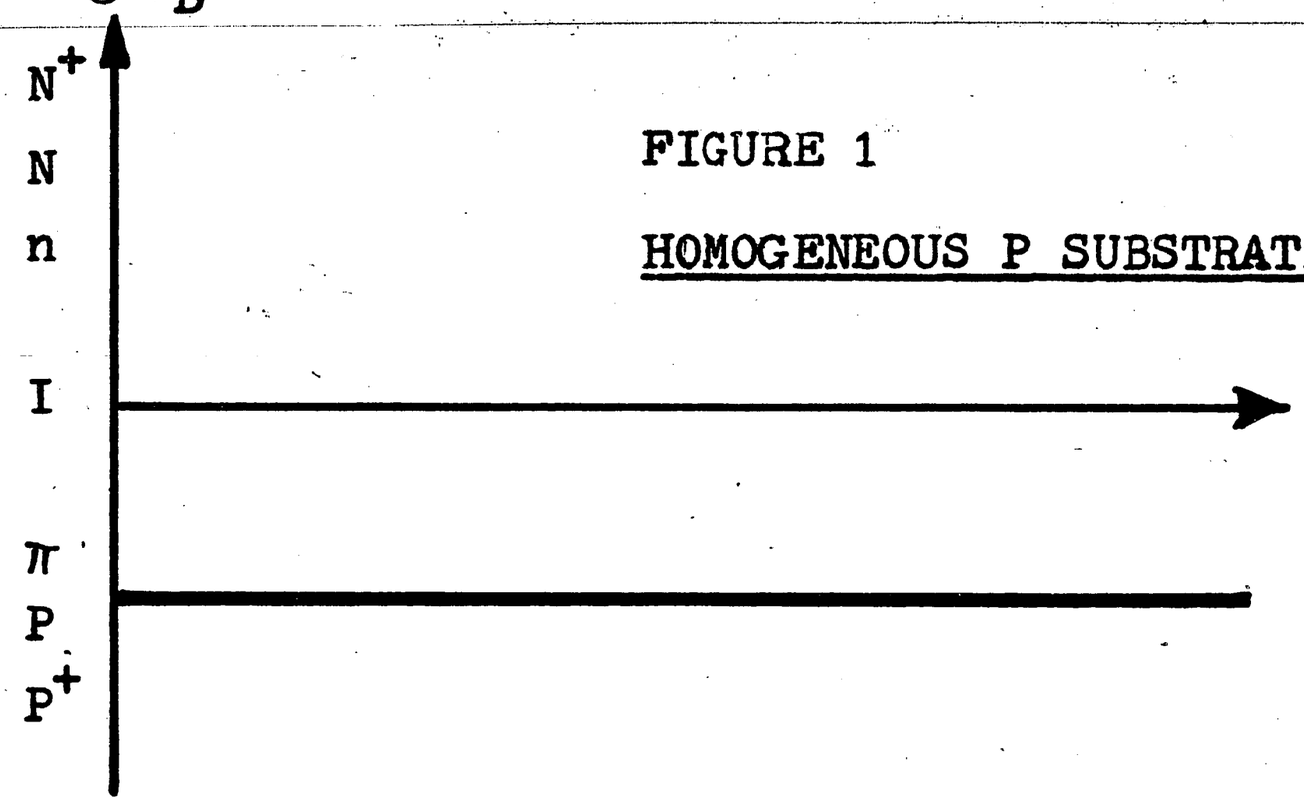


FIGURE 1

HOMOGENEOUS P SUBSTRATE

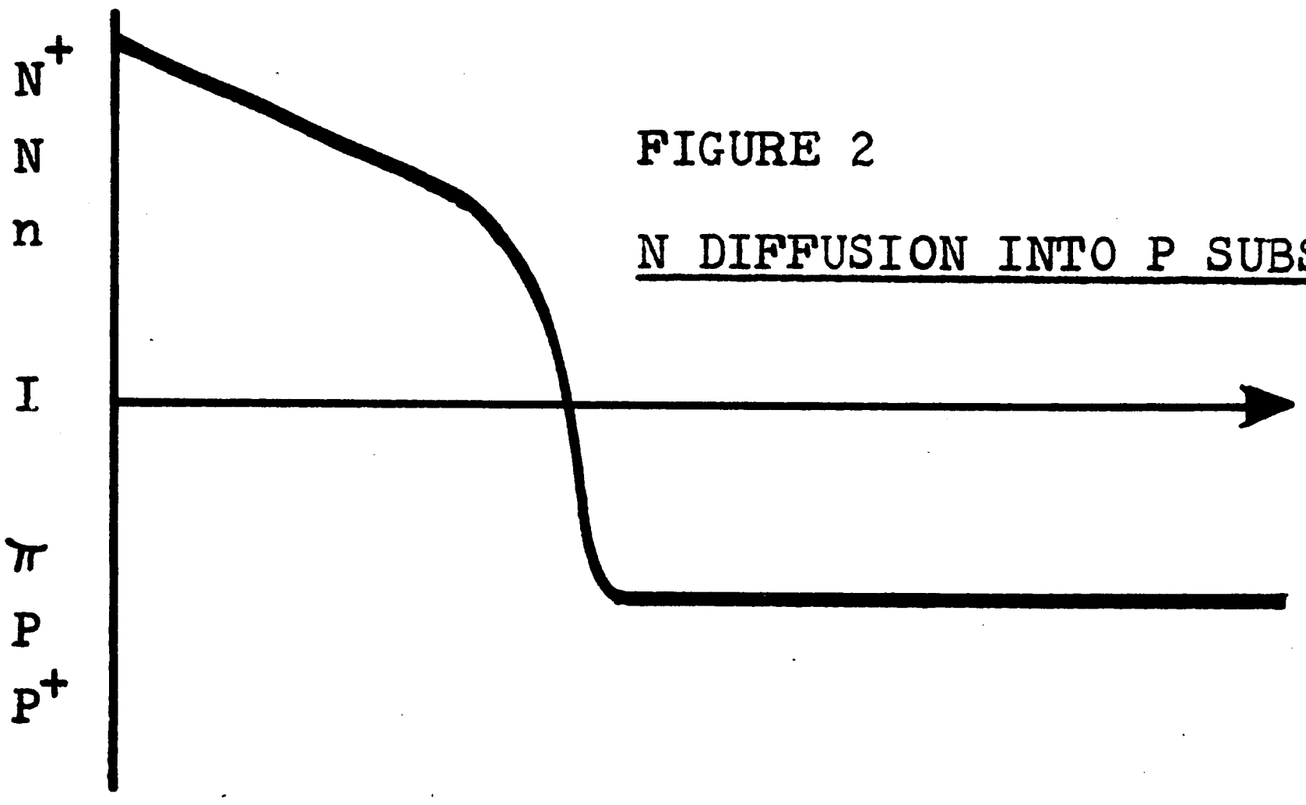


FIGURE 2

N DIFFUSION INTO P SUBSTRATE

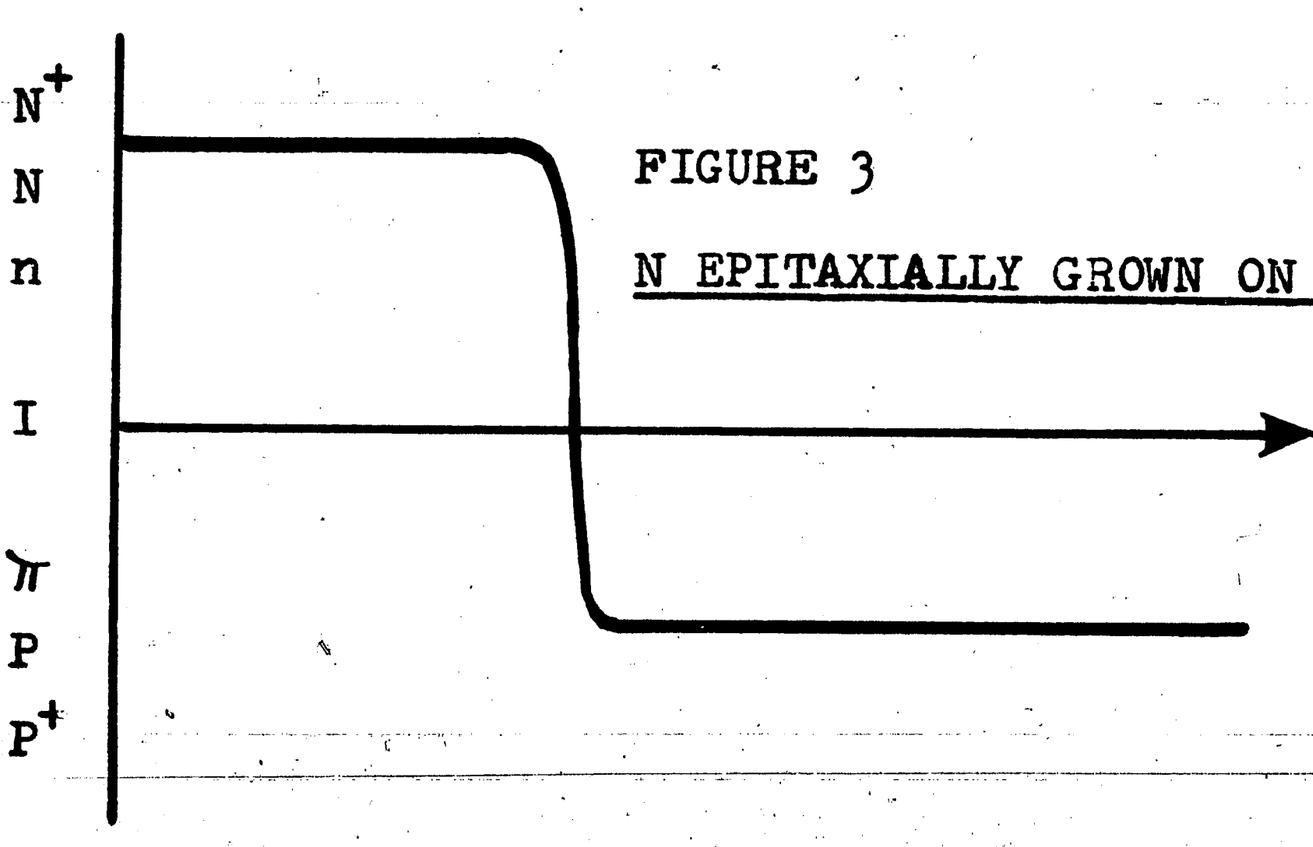


FIGURE 3

N EPITAXIALLY GROWN ON P SUBSTRATE

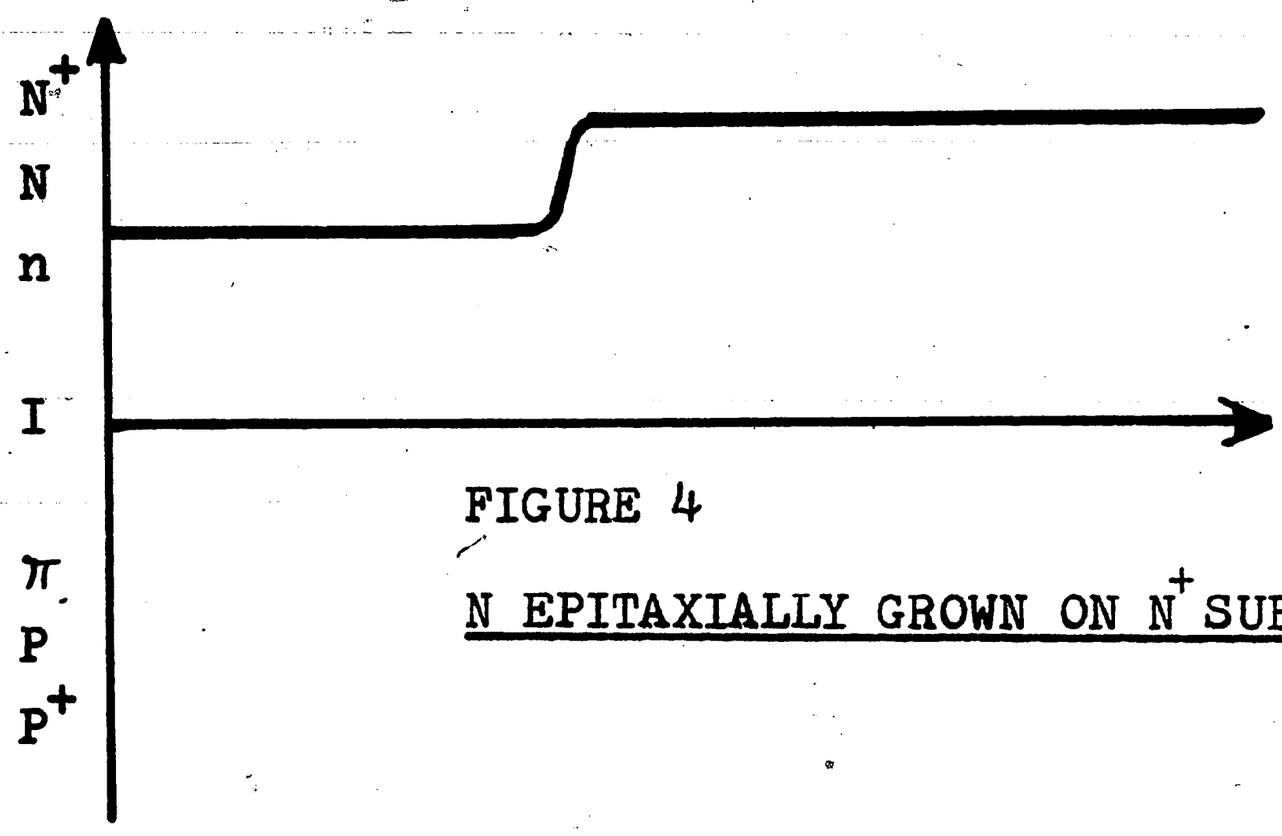


FIGURE 4

N EPITAXIALLY GROWN ON N^+ SUBSTRATE

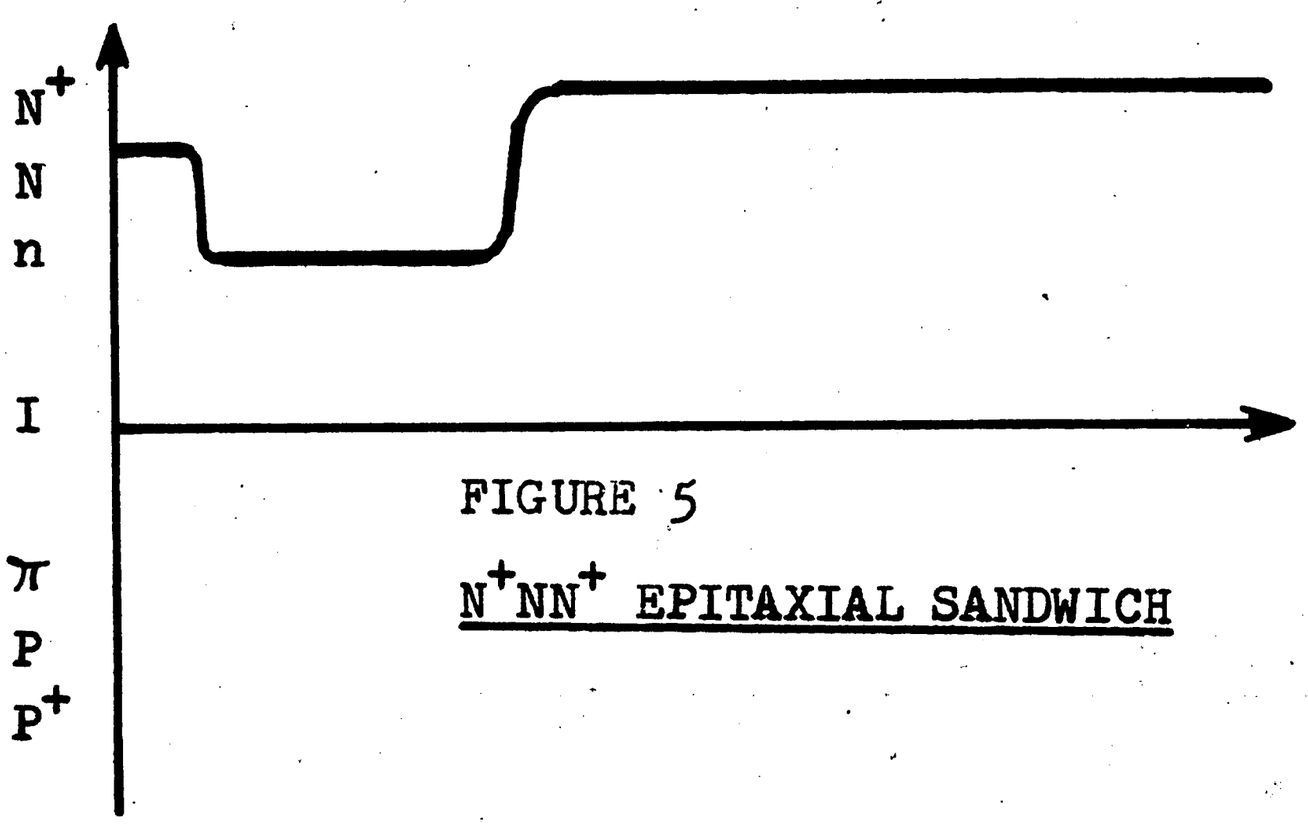


FIGURE 5

N^+NN^+ EPITAXIAL SANDWICH

an N^+ (or heavily doped N type) wafer. This is a popular doping profile used where lightly doped (few impurities) material is required at the surface to form devices with high breakdown voltages, low capacitances, etc.; but where low resistivity, highly doped material is needed in the bulk to minimize the series resistance of the devices.

Figure 5 shows one of the many unusual doping profiles which can be developed for special applications. This profile is used in microwave diodes to obtain an extremely rapid change in depletion layer width for small changes in bias voltage.

It would be helpful at this point to outline some of the methods previously developed for measuring doping profiles. Each method has its own advantages and drawbacks. The "best" method in any particular situation depends on the equipment available, the accuracy required, the type of profile being measured, and the amount of time available for measurement.

The oldest and most popular method for measuring doping profiles on semiconductor wafers involves measuring resistivity by the 4 point probe method (see figure 6). A constant current is passed through the outer two probes and the resulting electric field is measured between the inner two probes. This potential is proportional to the resistivity of the

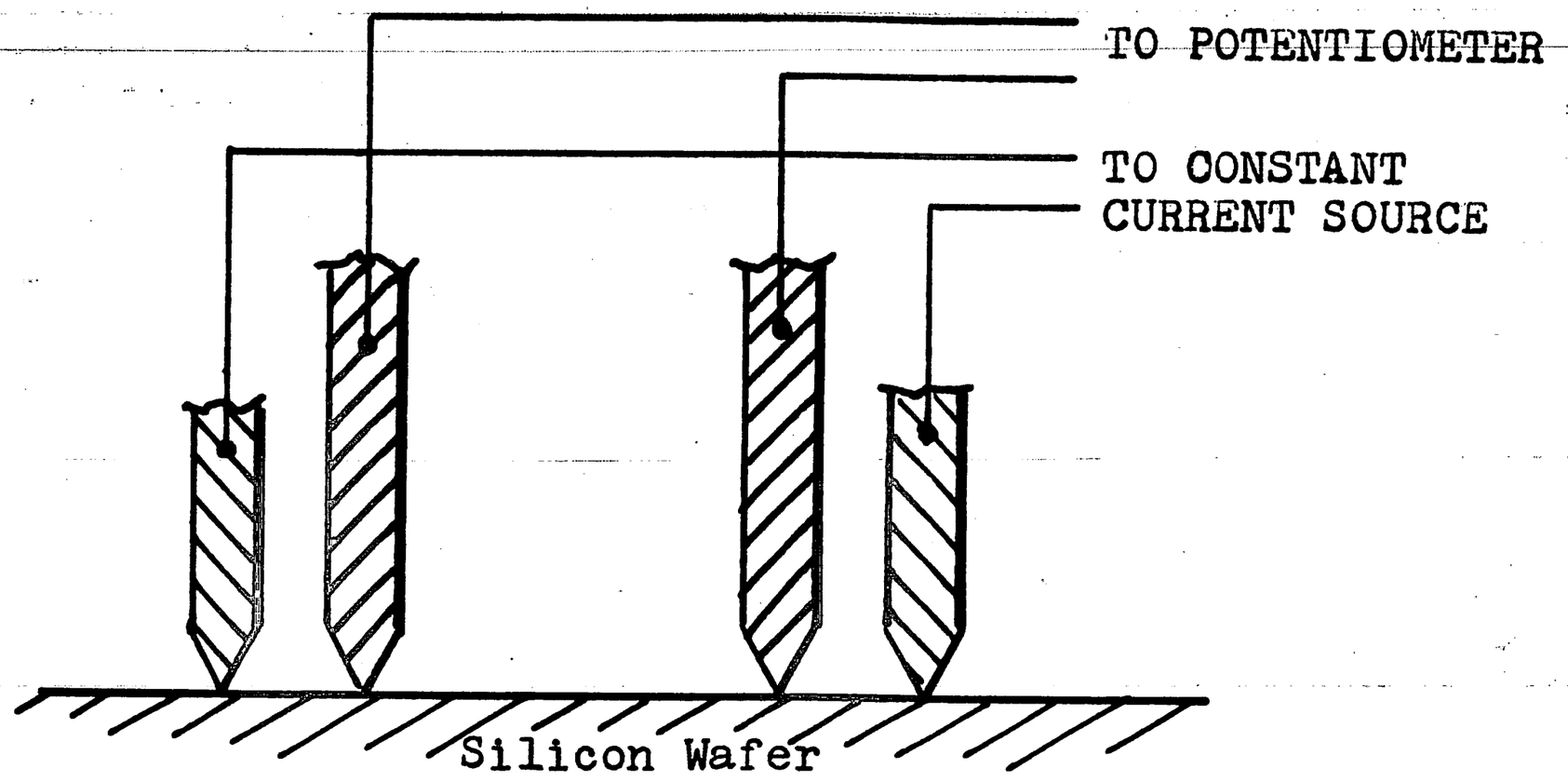


FIGURE 6

NORMAL 4 POINT PROBE CONFIGURATION

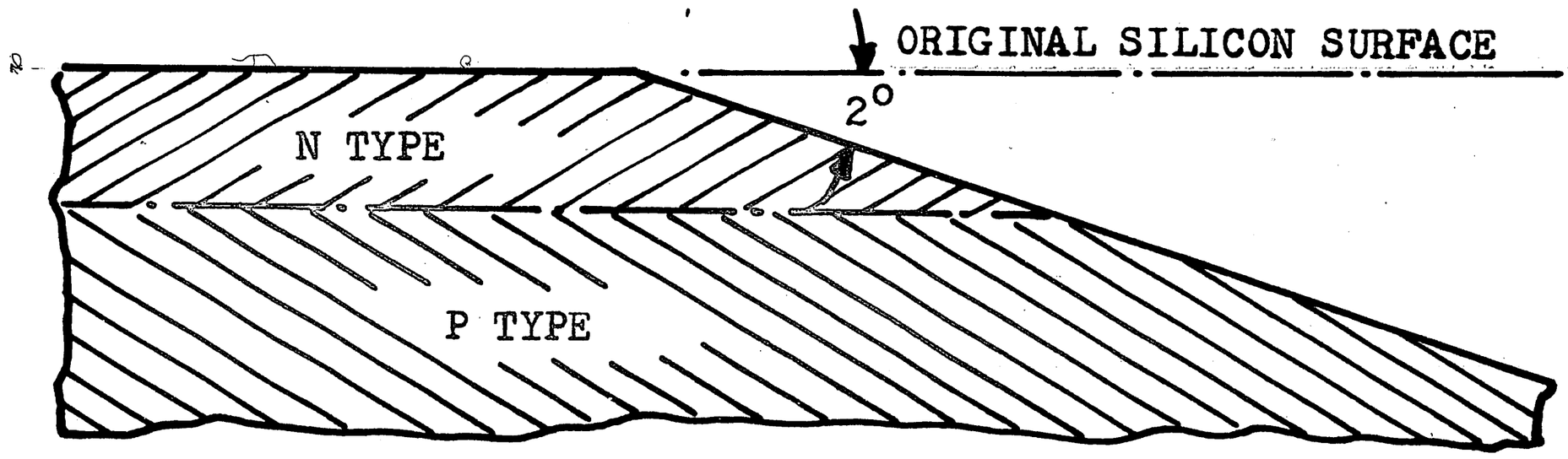


FIGURE 7

CROSS SECTION OF LAPPED WAFER

silicon near the surface; and, by using equations derived for most practical geometries, the bulk or surface resistivity (depending on the nature of the sample) can be calculated directly from the potential measurements.(31)

The impurity density can now readily be determined from experimentally determined plots of resistivity versus doping level.(12) This method works best on homogeneous material such as shown in figure 1. In this case the doping level is calculated directly from one simple measurement.

If, however, the doping is not uniform the job is harder. The resistivity profile may now be found by first lapping the wafer as shown in figure 7, either mechanically or by anodic etching.(25, 29) The surface resistivity is now measured as before with the four probes at regular intervals along the lapped region. The resistivity can now be plotted as a function of depth and the derivative of this curve can be directly related to the impurity density as a function of depth. (7,29)

As might be guessed from the above description, using the 4 point probe method to measure profiles on non-uniformly doped wafers is a long tedious operation. Also, this method can not be used effectively on many popular types of profiles (see for example the NN^+

profile of figure 4) because the resistance effect being measured is masked out by leakage and other error effects.(15, 26, 34)

Many variations of the 4 point probe method have been developed to overcome some of its drawbacks. For example, the four point over under method and the two point method were developed to permit reasonably accurate measurements on NN^+ or PP^+ materials (see figure 8 for probe configuration).(28) The three point spreading resistance method uses fewer probes and thus permits measurement on a smaller area of the wafer. Several ways of grinding, etching, or lapping the wafer have been developed.(8, 9, 17, 25, 29)

In contrast to these resistance measurement methods, there are a group of measurement techniques which utilize the relationship between the width of the depletion layer formed at the P-N junction and the impurity profile. These include the punch-through voltage method (27), the diode breakdown method(27), the MOS capacitance method (14), and several junction capacitance methods.(10, 11, 19, 30)

The punch-through voltage method uses two probes at the surface of the wafer (figure 9).(27) When a voltage is applied across the two probes, a charge depletion region is formed directly below one of the rectifying junctions formed by the metal-semiconductor

FIGURE 8

4 POINT OVER UNDER PROBE CONFIGURATION

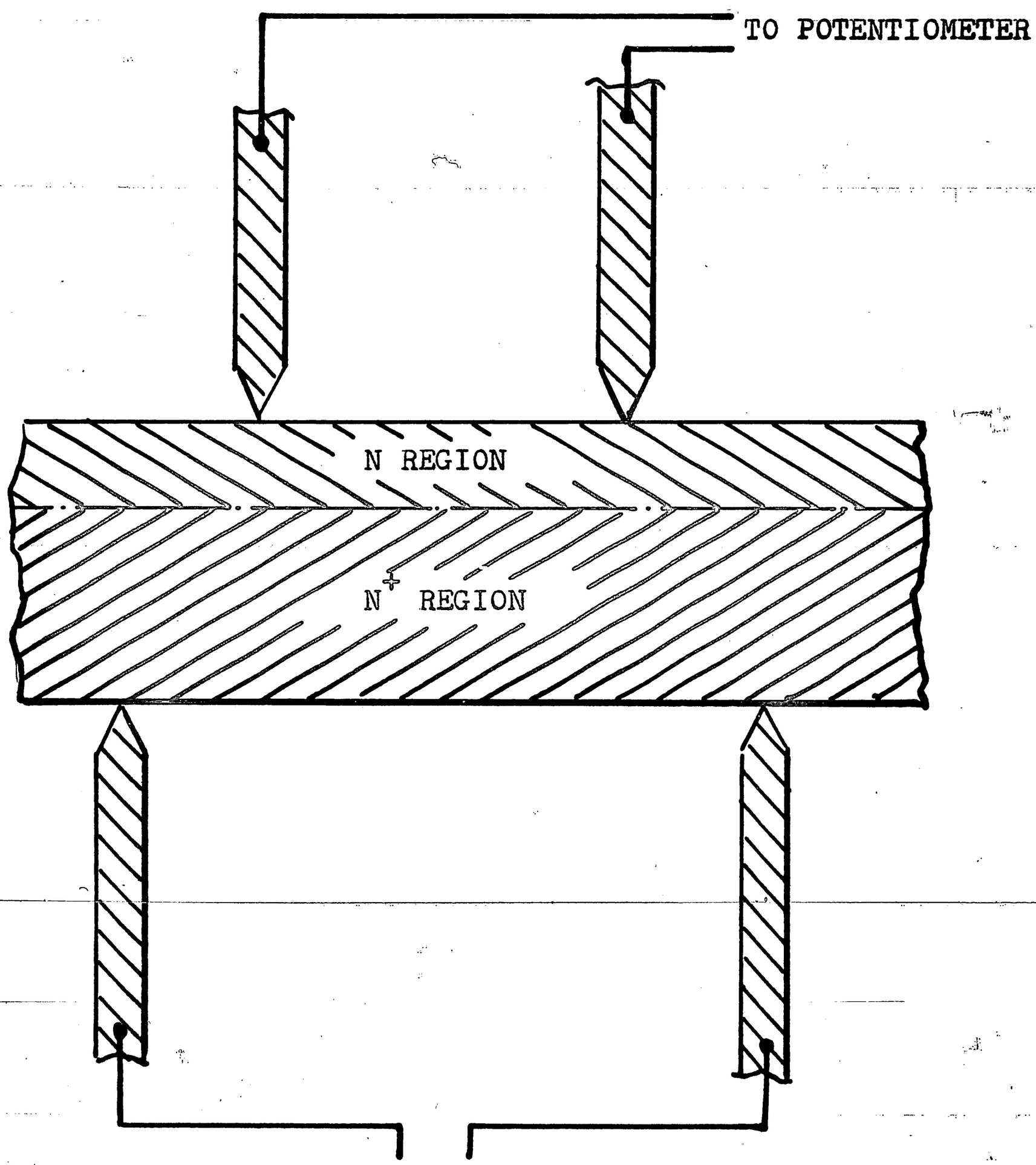
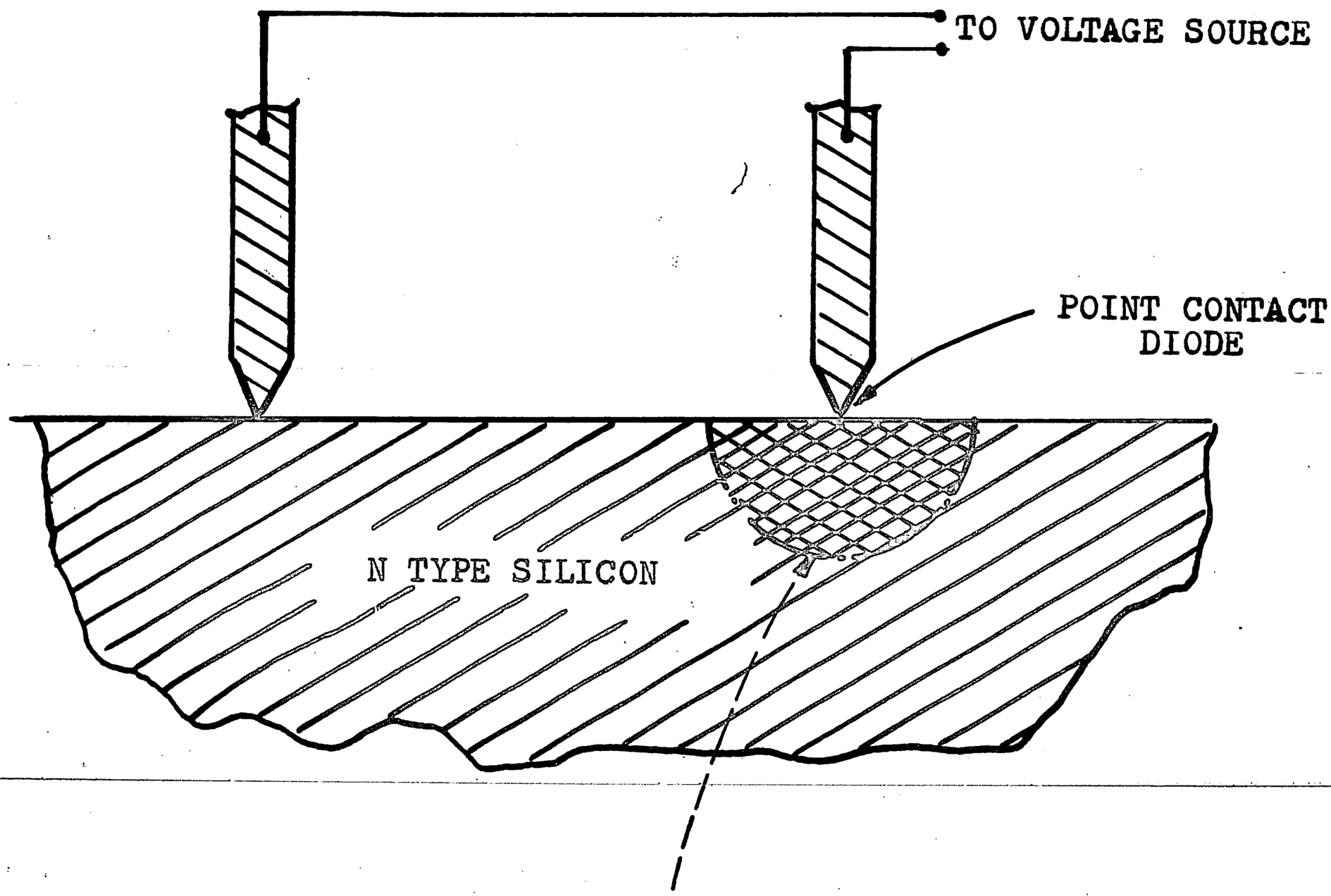


FIGURE 9

PUNCH THROUGH VOLTAGE METHOD



DEPLETION REGION SPREADING INTO SILICON
WITH POINT CONTACT DIODE UNDER REVERSE BIAS

contact.(3) If the silicon is uniformly doped, the voltage which can be supported across this depletion region depends only on the width of the depletion region which in turn can be related to the doping density.(30) The relation between the punch-through voltage of this rectifying contact and the doping density can either be calculated or determined experimentally. If the doping is not uniform the procedure becomes more complicated, requiring a lapping process to expose the various layers of the wafer as is done for the four point probe method. Also the depletion region can extend as much as thirty microns from the point of contact into the material. Therefore, if the region of interest is less than thirty microns thick and the depletion layer spreads through several regions of different doping levels, then the punch-through voltage no longer depends only on the average impurity density, but on a whole group of complicated factors. Analysis under these conditions is impossible and the method thus becomes impractical.

The diode breakdown voltage method is similar to the punch-through voltage method.(27) Here biasing a planar diode produces the same depletion layer that was formed under the point contact diode in the punch-through method. The analysis is made easier by the planar configuration of the diode but measurement of

a non-uniformly doped wafer is still difficult. One is still plagued by the need to lap the surface of the wafer and analysis still is not possible unless the impurity density is reasonably uniform over the width of the depletion region.

The junction capacitance versus voltage method is the most promising method yet developed for measuring the impurity profile on non-uniformly doped wafers. It enables measurements to be made of impurity density as a function of x, the distance from the surface of the wafer, as deep as 30 or 40 microns without lapping, etching, or otherwise destroying the wafer.

The depletion layer capacitance of a planar P-N junction is given as:

(#1) $$C = \frac{\epsilon A}{W}$$

where

ϵ = Dielectric Constant of Semiconductor

C = Junction Capacitance

A = Junction Area

W = Width of Depletion Region

The exact relation between junction capacitance and voltage will be derived for an arbitrarily doped wafer.(10, 23, 30)

Let us apply a small increment of voltage, ΔV,

to the junction. The change in the electric field is then

(#2) $$\Delta E = \frac{\Delta V}{W}$$

The increment of charge per unit area required to produce this field is

(#3) $$\frac{\Delta Q}{A} = \epsilon \Delta E = \frac{\epsilon \Delta V}{W}$$

(#4) $$C = \frac{\Delta Q}{\Delta V} = \frac{\epsilon A}{W}$$

Since W is a function of voltage the chain rule can be used to show:

(#5) $$\frac{dC}{dV} = \frac{d}{dV}\left(\frac{\epsilon A}{W}\right) = \frac{d}{dW}\left(\frac{\epsilon A}{W}\right)\frac{dW}{dV} = \frac{-\epsilon A}{W^2}\frac{dW}{dV}$$

The amount of charge swept out of the incremental volume by the incremental potential is:

(#6) $Q = qN_D A \Delta W_D$ on the N side

(#7) $Q = qN_A A \Delta W_A$ on the P side

where

N_D = N Type Impurity or Doping Density

N_A = P Type Impurity or Doping Density

(#8) $$\Delta W = \Delta W_A + \Delta W_B = \frac{\Delta Q}{qN_A A} + \frac{\Delta Q}{qN_D A} = \frac{\Delta Q}{qA}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)$$

From equation #4

(#9) $$\frac{\Delta W}{\Delta V} = \frac{\epsilon}{Wq}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)$$

Equation #9 can now be substituted back into equation #5 and equation #4 used to get:

$$(\#10) \qquad \frac{dC}{dV} = \frac{-\epsilon^2 A}{W^3 q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) = \frac{C^3}{q\epsilon A^2}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)$$

Now, for example, if the impurity profile of some non-uniformly doped N type wafers is to be measured, a thin but highly doped P region is first thermally formed on the wafer surface. Using either aluminum or boron as the P type impurity, we can insure that the P type impurity density is higher than the highest impurity density that might exist in the N type wafer being measured. The area of the P type layer is accurately measured and is approximately equal to the junction area. Knowing A and given that

$$(\#11) \qquad N_A \gg N_D \Rightarrow \frac{1}{N_A} \ll \frac{1}{N_D}$$

a simpler form of equation #9 can be obtained:

$$(\#12) \qquad N_D(W) = \frac{C_0^3}{q\epsilon A^2 \left.\frac{dC(V)}{dV}\right|_{V_0}}$$

Since q and ϵ are known constants, the problem reduces to that of measuring C and $\frac{dC}{dV}$ as functions of voltage. The most straight forward approach is to measure and plot C versus V.(19, 30) The derivative can be computed graphically and $\frac{dC}{dV}$ plotted as a

function of voltage. Using equations #3 and #10, points can be picked off these two curves to determine N_D versus W. The primary disadvantage to this system is that it requires a great deal of time and that much accuracy is lost when taking the derivative of the C(V) curve.

In another approach a P-N junction is formed as described above and then the current spike resulting from the application of a sharp step voltage across the junction is integrated (figure 10) to obtain the total displaced charge, Q_t.(10) The amplitude of the voltage step function, V, can be automatically swept between 0 and V_B. At the same time, a small high frequency A-C voltage is added on top of the voltage step function and the A-C current through the diode is measured. The elastance of the diode is given as

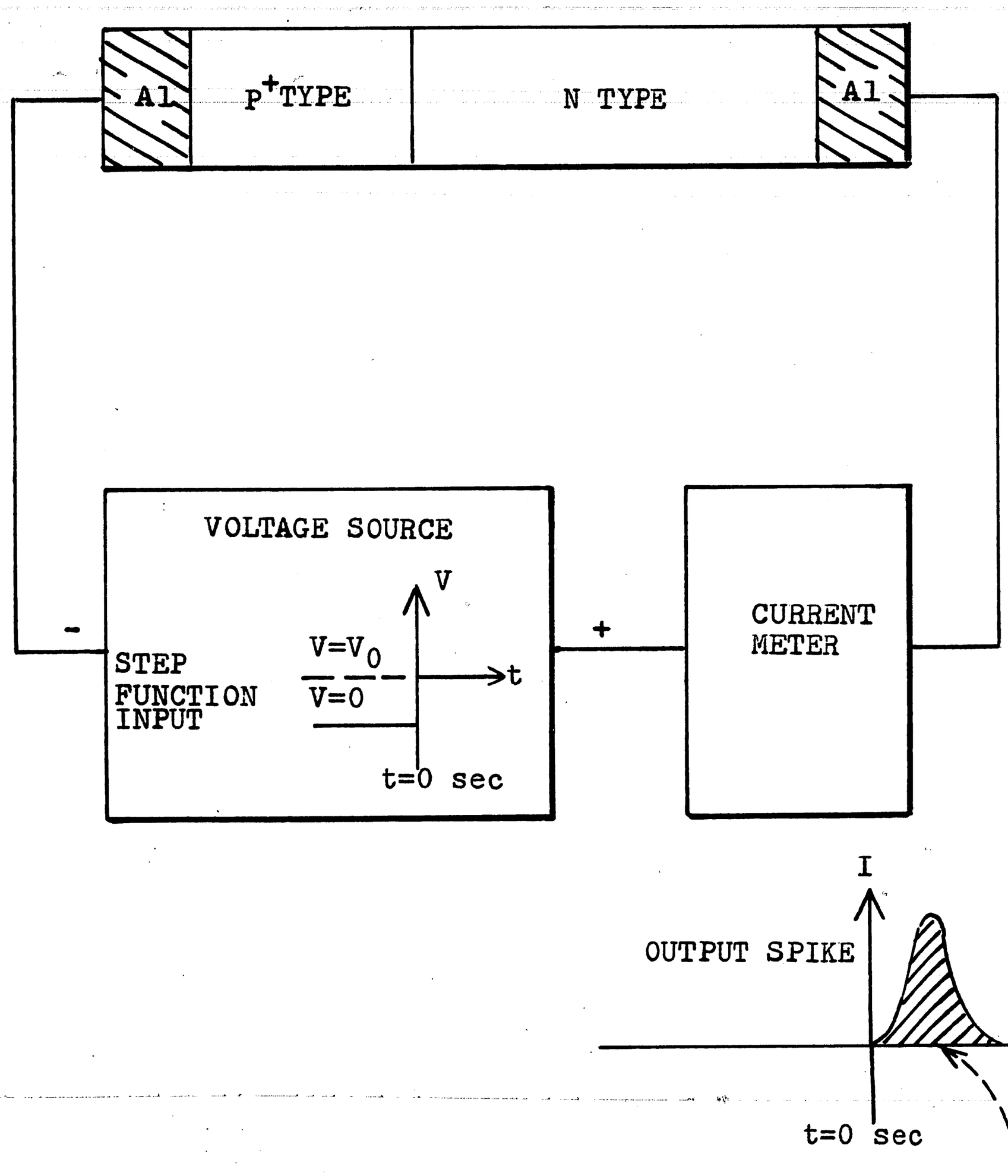
(#13) $$S = \frac{1}{C} = \frac{V_{A-C}}{I_{A-C}} = \frac{W}{\epsilon A}$$

So W = x, the distance the depletion width extends into the wafer, is simply proportional to the reciprocal of the output A-C current and can be measured continuously and automatically as a function of V.

Both outputs are fed into a curve tracer where Q_t versus W is plotted as V swings between 0 and V_B. Using equation #8, N_D and $\frac{dQ_t}{dW}$ are simply related if $N_A \gg N_D$.

FIGURE 10

CHARGE STORAGE METHOD



(#14) $$\frac{dQ_t}{dW} = \frac{qA}{\frac{1}{N_A} + \frac{1}{N_D}} = qAN_D$$

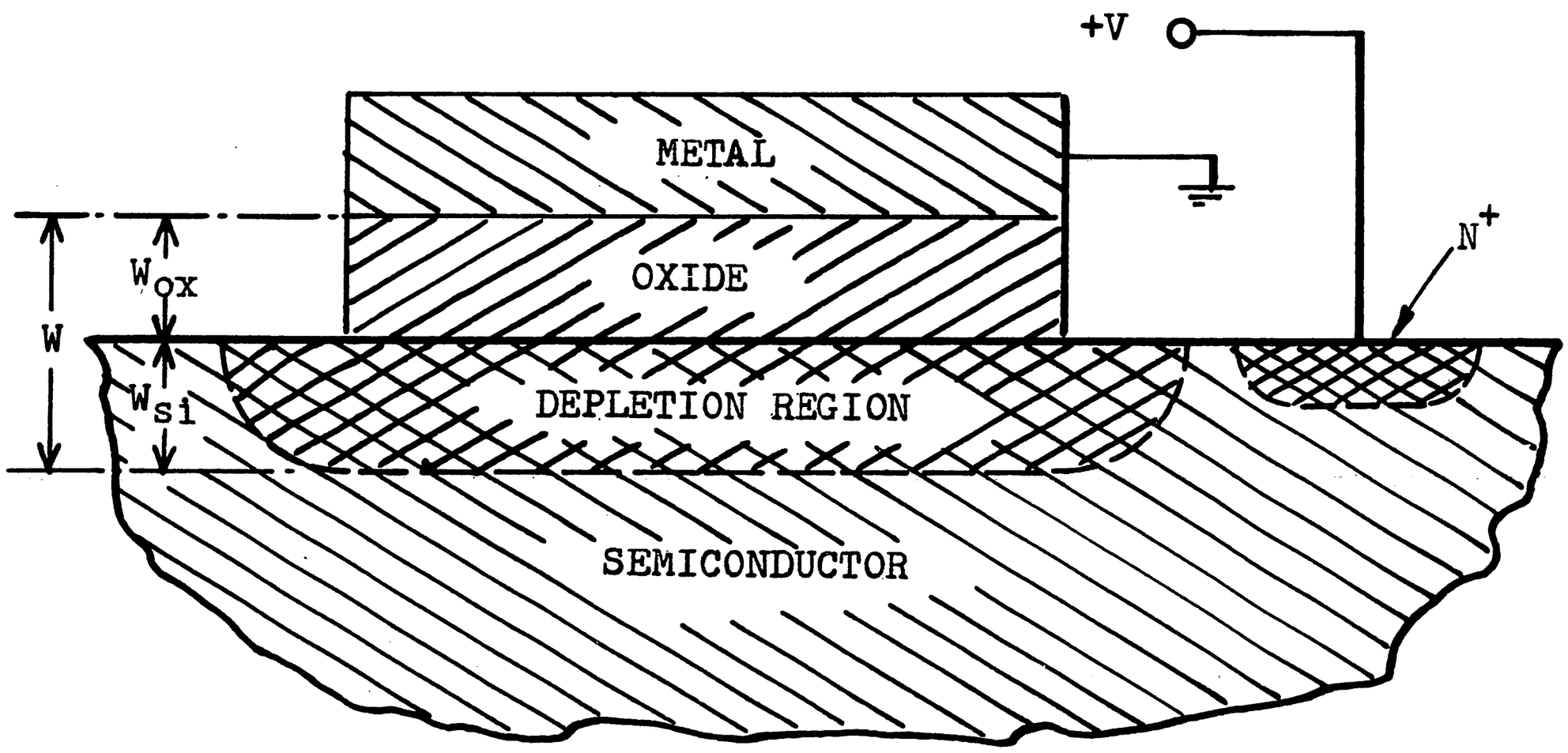
Thus a plot of N_D versus W may be obtained from the derivative of the Q_t versus W plot. The circuitry required for doing this automatically is relatively simple, so that the required profile can be displayed instantaneously on a curve tracer, thus eliminating the tedious labor described in the previous method. However, this method still suffers from the magnification of errors when the derivative of the Q_t versus V curve is taken.

A third approach utilizing the depletion layer capacitance effect is to measure the incremental change in capacitance, $\frac{dC}{dV}$, directly as a function of bias voltage. This is the method considered in this paper and will be discussed at the end of this section.

Several other measurement techniques are closely related to the depletion layer capacitance methods. The metal-oxide-semiconductor method is similar to the three junction capacitance methods previously discussed except that it utilizes a metal-oxide structure instead of a junction to produce the depletion layer (figure 11).(14) The C(V) and $\frac{dC}{dV}$ (V) curves are plotted versus W as before, but now the thickness of the oxide, W_{ox}, must be subtracted from the apparent depletion width to get the true

FIGURE 11

MOS CAPACITANCE METHOD



width, W_{si}, of the depletion layer.

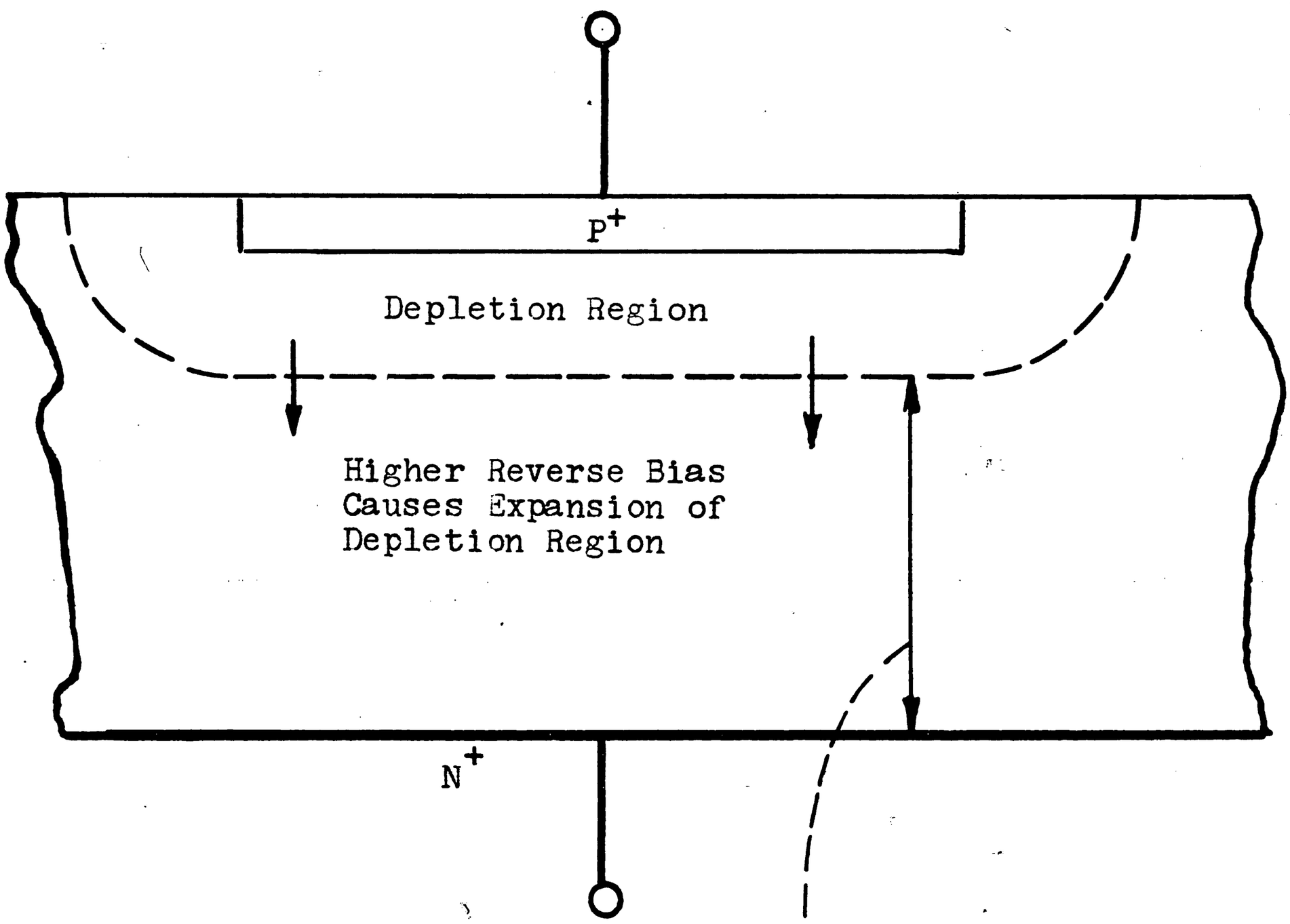
(#15) $$W_{si} = W - \frac{\epsilon_{si}}{\epsilon_{ox}} W_{ox}$$

After the measurement has been made, the metal and oxide can be etched away leaving the silicon surface as it was before the measurements were made. Thus we avoid the irreversable diffusion, sintering, or alloying process required for the junction capacitance methods. This method suffers, however, from a loss in sensitivity and accuracy due to the oxide thickness, W_{ox}.

Another significant alternative is to back bias a P-N junction as before and measure the series resistance appearing in series with the depletion layer capacitance instead of the capacitance itself. When a current passes into the capacitor it must pass through the wafer to the edge of the depletion region where the charge is stored (see figure 12). As the depletion region expands into the N material the effective thickness of the relatively high resistance N material region decreases. Thus, the series resistance will decrease as the bias voltage is increased. So, if R versus V and $\frac{dR}{dV}$ versus V are found, the impurity profile of the wafer can be calculated. However, this method can be expected to be reasonably sensitive only when used on NN^+ or PP^+ type profiles

FIGURE 12

RESISTANCE VARIATION IN P-N JUNCTIONS



and even here the resistance is not typically as sensitive a function of bias voltage as is capacitance (figure 13).(20)

Radioactive tracing is a direct method of measuring impurity profiles. The change in radioactivity of the sample is measured as layers of the wafer are successively etched away. A series of sample control wafers can also be used as a direct measure of impurity profiles.

The third depletion layer capacitance method - measuring $\frac{dC}{dV}$ directly by harmonic analysis - is discussed in detail in this paper. This technique measures the voltage generated at the second harmonic when a small A-C voltage is impressed across the diode junction.

In the next section the theory behind this method will be presented. It will be shown that, with a constant small input voltage;

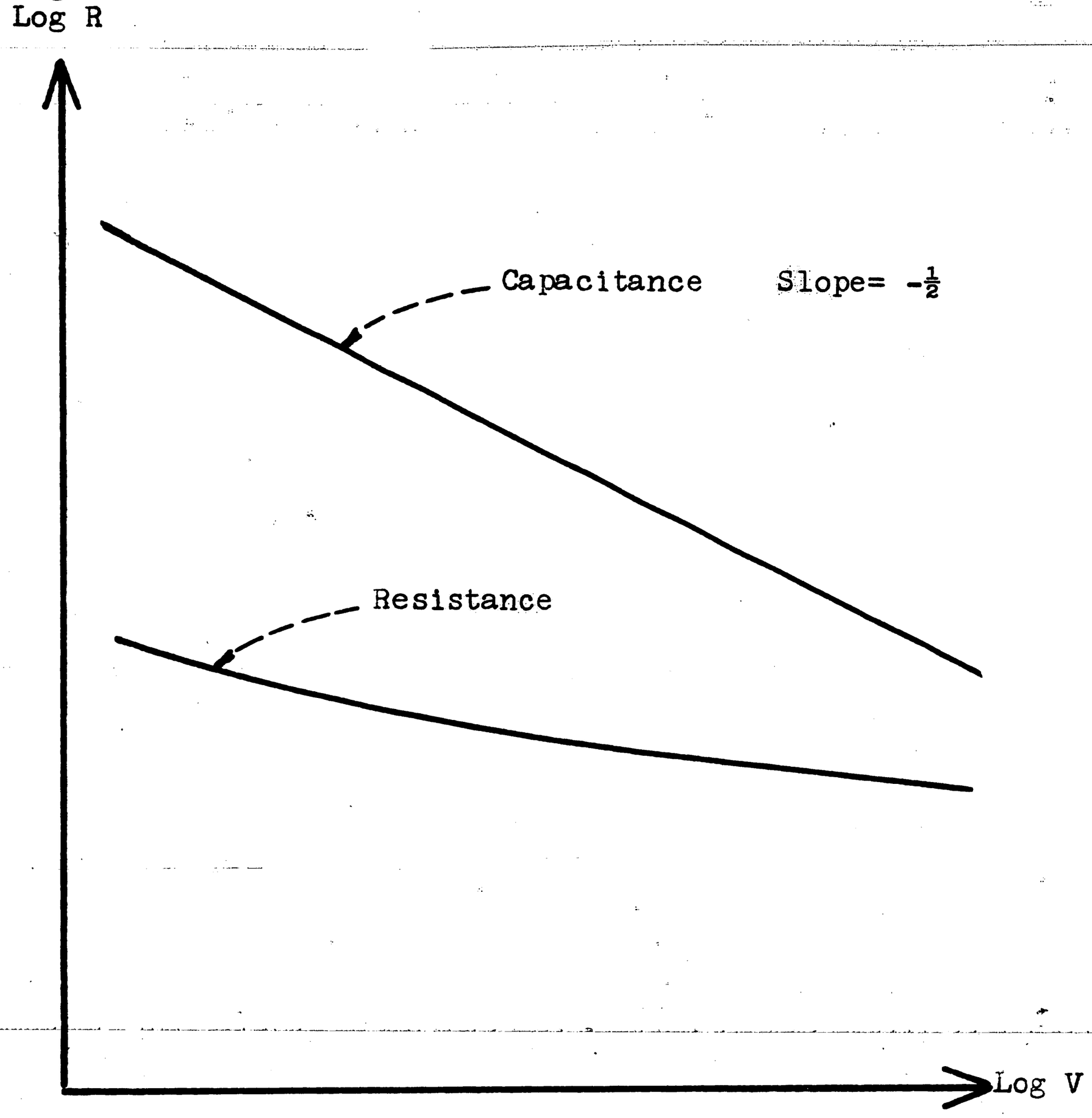
(#16) $$\left[V_{out}(\text{Fundamental})\right] \sim C$$

(#17) $$\left[V_{out}(2^{nd}\ \text{harmonic})\right] \sim \frac{dC}{dV}$$

In the third section, the experiments performed on a planar P I N diode will be presented and discussed. Finally, a discussion of experimental results and an evaluation of the merits of this new method will be presented in the conclusion.

FIGURE 13

TYPICAL C(V) AND R(V) RELATIONS FOR A N ON N^+ WAFER



Theory

In this section, two important relationships will be derived. The first relationship is between the voltage at the second harmonic frequency and $\frac{dC}{dV}$. The second important relationship is between the voltage at the fundamental frequency and C(V).

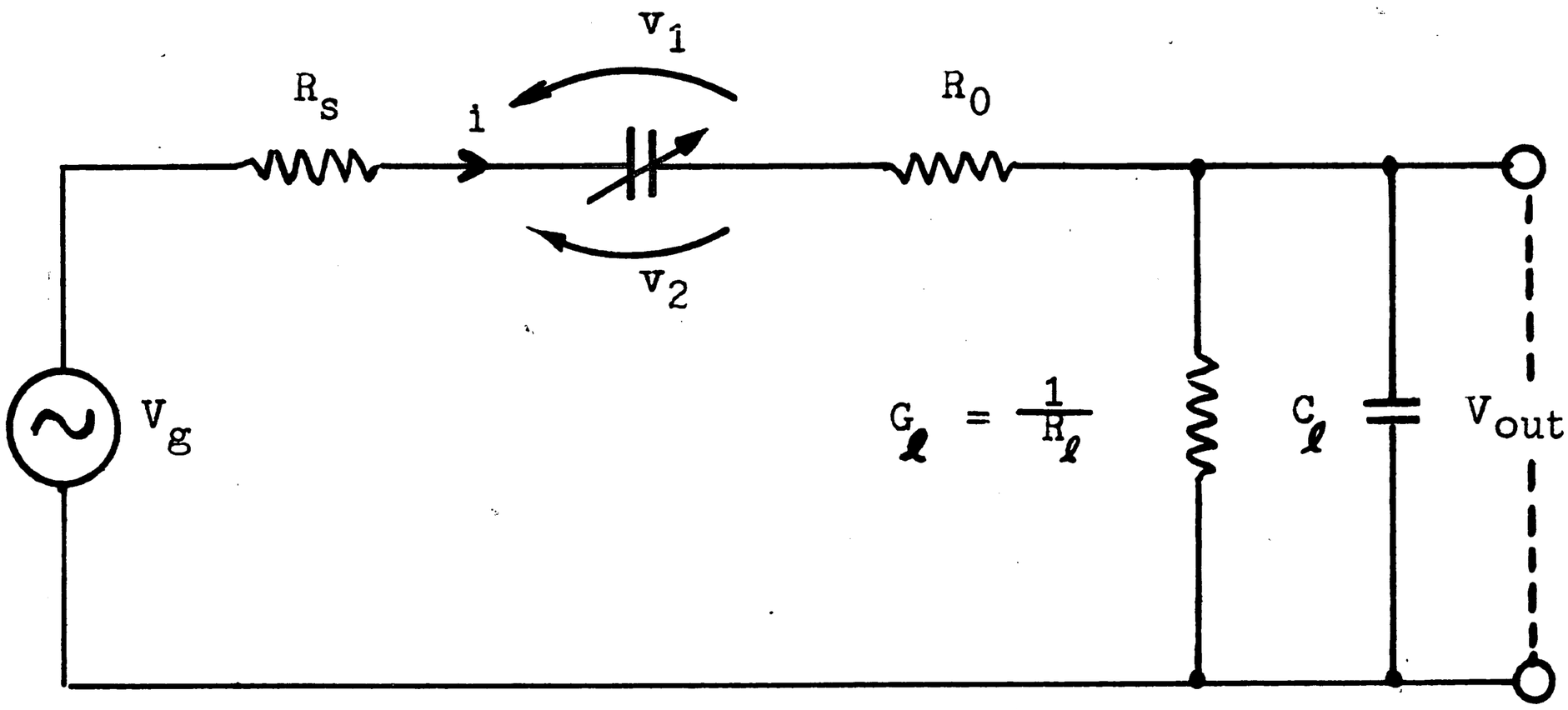
The diode is used in the following experimental circuit (see figure 14). The circuit is driven by an A-C signal source, V_g, shown with its internal resistance, R_s. The diode is modeled as a variable capacitance in series with the line. The series resistance of the diode, though variable, is always small (< 10) and thus negligible. R_0 is a resistance which can be added in series with the diode. The load is represented by the parallel combination of a termination resistance, R_L, and the capacitive input of the preamplifier.

The first step is to derive an expression for the depletion layer capacitance as a function of voltage and time. For any continuous capacitance versus voltage relation, the capacitance at any voltage, V_t, can be expressed in terms of the capacitance at some bias point, V_0, by a Taylor expansion.

(#18) $$C(V_t) = C(V_0) + \frac{dC}{dV}(V_t - V_0) + \text{etc.}$$

FIGURE 14

DIODE CIRCUIT



This analysis will be restricted to cases where the bias voltage (V_0) is large compared to the amplitudes of the A-C signals (V_1, V_2, etc.) so that:

(#19) $$V_0 \gg V_1 > V_2 > V_3 > V_4 \quad \text{etc.}$$

This permits a simplification of equation #18 as only the first two terms of the Taylor series need to be considered - the other terms being negligibly small.

The voltage, V_t, across the diode can be expressed as a function of time and the amplitudes of the A-C signals:

(#20) $$V_t = V_0 + V_1\cos\omega t + V_2\cos\omega t + \text{etc.}$$

The theory is, at this point, further limited to cases where the amplitude of the fundamental is much greater than the amplitude of any other frequency.

(#21) $$V_0 \gg V_1 \gg V_2 > V_3 > V_4 \quad \text{etc.}$$

This permits the following small-signal approximation of equation #20.

(#22) $$V_t = V_0 + V_1\cos\omega t = V_0 + \alpha V_0\cos\omega t$$

where $$\alpha = \frac{V_1}{V_0} .$$

Substituting equation #22 into equation #18

yields:

$$(\#23)\quad C(V_0,t) = C(V_0) + \alpha V_0 \left.\frac{dC(V)}{dV}\right|_{V_0} \cos\omega t$$

$$= C(V_0)\left[1 + \frac{\alpha V_0 \left.\frac{dC(V)}{dV}\right|_{V_0} \cos\omega t}{C(V_0)}\right]$$

$$= C(V_0)\left[1 + \frac{\alpha V_0 \left.\frac{dC(V)}{dV}\right|_{V_0}}{2C(V_0)}(e^{j\omega t} + e^{-j\omega t})\right]$$

Equation #23 can be rewritten in the following form:

$$(\#24)\quad C(V_0,t) = C_0\left[1 + \frac{\gamma_1}{2}(e^{j\omega t} + e^{-j\omega t})\right]$$

where $\gamma_1 = \dfrac{V_1 \left.\frac{dC(V)}{dV}\right|_{V_0}}{C_0}$

and $0 = \gamma_2 = \gamma_3 = \gamma_4$ etc.

The fundamental and second harmonic frequency voltages across the diode can be expressed as follows:

$$(\#25)\quad v_1 = V_1 e^{j\omega t} + V_1^* e^{-j\omega t}$$

$$(\#26)\quad v_2 = V_2 e^{j2\omega t} + V_2^* e^{-j2\omega t}$$

Expressing C as a function of v_1,

$$(\#27)\quad C(v_1) = v_1 \left.\frac{dC(V)}{dV}\right|_{V_0} + C_0$$

$$(\#28)\quad C(v_1) = C_0 + V_1 \left.\frac{dC(V)}{dV}\right|_{V_0} e^{j\omega t} + V_1^* \left.\frac{dC(V)}{dV}\right|_{V_0} e^{-j\omega t}$$

$$(\#29)\quad i = I_1 e^{j\omega t} + I_1^* e^{-j\omega t} + I_2 e^{j2\omega t} + I_2^* e^{-j2\omega t}$$

It is now possible to apply the results of a general large signal harmonic analysis derived in Blackwell and Kotzebue.(4) Substituting n = 2 for the second harmonic in equation 4.86, the matrix equations are

$$(\#30)\quad I_1 = j\omega C_0 [1 - \gamma_2] V_1 + j\omega C_0 \gamma_1 V_2$$

$$(\#31)\quad I_2 = j\omega C_0 [\gamma_1 - \gamma_3] V_1 + j2\omega C_0 V_2$$

where γ_1, γ_2, and γ_3 are the fractional variations in C due to the fundamental, second, and third harmonic frequencies respectively.

Using equation #24

$$(\#32)\quad I_1 = j\omega C_0 (V_1 + \gamma_1 V_2)$$

$$(\#33)\quad I_2 = j\omega C_0 \gamma_1 V_1 + j2\omega C_0 V_2$$

From equations #20 and #21, $\gamma_1 \ll 1$ and $V_2 \ll V_1$ making it possible to neglect $\gamma_1 V_2$ compared to V_1 as a second order effect. Again, using equation #24,

$$(\#34)\quad I_1 = j\omega C_0 V_1$$

$$(\#35)\quad I_2 = j\omega V_1^2 \left.\frac{dC(V)}{dV}\right|_{V_0} + j2\omega C_0 V_2$$

From figure 14 the relation between V_2 and I_2 can be determined.

$$(\#36)\quad V_2 = I_2\left(R_s + R_0 + \frac{1}{j2\omega C_\ell + G_\ell}\right) = I_2 Z_2$$

Equation #35 now becomes

$$(\#37)\quad \frac{V_2}{Z_2} = j\omega V_1^{\,2}\left.\frac{dC(V)}{dV}\right|_{V_0} = j2\omega C_0 V_2$$

$$(\#38)\quad V_2\left(\frac{1}{Z_2} - j2\omega C_0\right) = j\omega V_1^{\,2}\left.\frac{dC(V)}{dV}\right|_{V_0}$$

Voltages V_1 and V_2 are not directly measurable. Only the input voltage, V_g, and the output voltage, V_{out}, can be measured. It is necessary then to relate V_1 to V_g using figure 14:

$$(\#39)\quad V_1 = \frac{V_g}{j\omega C_0\left(R_s + R_0 + \frac{1}{j\omega C_\ell + G_\ell} + \frac{1}{j\omega C_0}\right)} = \frac{V_g}{j\omega C_0 Z_1}$$

$$(\#40)\quad V_2 = (j2\omega C + G_\ell)\left(R_s + R_0 + \frac{1}{j2\omega C + G_\ell}\right)V_{out} = \frac{Z_2}{Z_{L2}} V_{2out}$$

Combining equations # 38, #39, and #40,

$$(\#41)\quad V_{2out}\frac{Z_2}{Z_{L2}}\left(\frac{1}{Z_2} - j2\omega C_0\right) = \frac{j\omega V_g^{\,2}\left.\frac{dC(V)}{dV}\right|_{V_0}}{-\omega^2 C_0^{\,2} Z_1^{\,2}}$$

$$(\#42)\quad V_{2out} = \frac{V_g^{\,2}\left.\frac{dC(V)}{dV}\right|_{V_0}}{\frac{Z_1^{\,2}}{Z_{L2}}\omega C_0^{\,2}(j + 2\omega C_0 Z_2)}$$

For the general case described by equation #42, it is possible to express $\frac{dC(V)}{dV}$ in terms of easily measured circuit parameters.

$$(\#43)\quad \frac{dC(V)}{dV} = \frac{\omega C_0^{\,2} Z_1^{\,2}(j + 2\omega C_0 Z_2)}{Z_{L2}} \frac{V_{2out}}{V_g^{\,2}}$$

Referring back to the introduction and the discussion of measuring impurity profiles by the depletion layer capacitance and harmonic analysis, note that equation #43 is the required relationship between $\frac{dC}{dV}$ and the output voltage at the second harmonic mentioned in equation #17. The required relation between C and the output voltage at the fundamental frequency mentioned in equation #16 can be obtained from equations #34, #39, and figure 14 as follows:

$$(\#44)\quad V_{1out} = I_1 Z_{L1} = j\omega C_0 V_1 Z_{L1} = \frac{Z_{L1}}{Z_1} V_g$$

Solving now for C_0:

$$(\#45)\quad Z_1 = R_s + R_0 + Z_{L1} + \frac{1}{j\omega C_0} = Z_{L1}\frac{V_g}{V_{1out}}$$

$$(\#46)\quad C_0 = \frac{\frac{1}{j\omega}}{Z_{L1}\frac{V_g}{V_{1out}} - Z_L - R_s - R_0} = \frac{\frac{1}{j\omega}}{Z_L(\frac{V_g}{V_{1out}} - 1) - R_s - R_0}$$

Having derived the required equation, #43 and #46, it is possible to substitute back into equations #12 and #13 to find $N_D(V_0)$ and $W(V_0)$:

$$(\#47)\quad N_D(V_0) = \frac{Z_{L1}C_0}{q\epsilon A^2\omega Z_1^{\,2}(\,j + 2\omega C_0 Z_2)} \frac{V_g^{\,2}}{V_{2out}}$$

$$(\#48)\quad W(V_0) = \frac{\epsilon A}{C_0} = j\omega\epsilon A\left[Z_{L1}(\frac{V_g}{V_{1out}} - 1) - R_s - R_0\right]$$

Now N_D and W can both be measured directly as V_0 is varied from less than zero volts to the breakdown voltage of the junction. $N_D = f(W)$ can easily be plotted graphically or displayed automatically on an oscilloscope.

If the series resistors R_s and R_0 are made large compared to the impedence of the other elements of the circuit then

$$(\#49)\quad \frac{1}{j2\omega C_0} < \frac{1}{j\omega C_0} \ll Z_1 \approx R_g + R_0 \approx Z_2 \gg Z_{L1} > Z_{L2}$$

Equations #43 and #47 can now be greatly simplified.

$$(\#50) \qquad \left.\frac{dC(V)}{dV}\right|_{V_0} = \frac{2\omega^2 C_0^{\,3}(R_s + R_0)^3}{Z_{L2}} \frac{V_{2out}}{V_g^{\,2}}$$

$$(\#51) \qquad N_D(V_0) = \frac{V_g^{\,2} Z_{L2}}{2q\epsilon A^2 \omega^2 (R_s + R_0)^3 V_{2out}}$$

Experiment

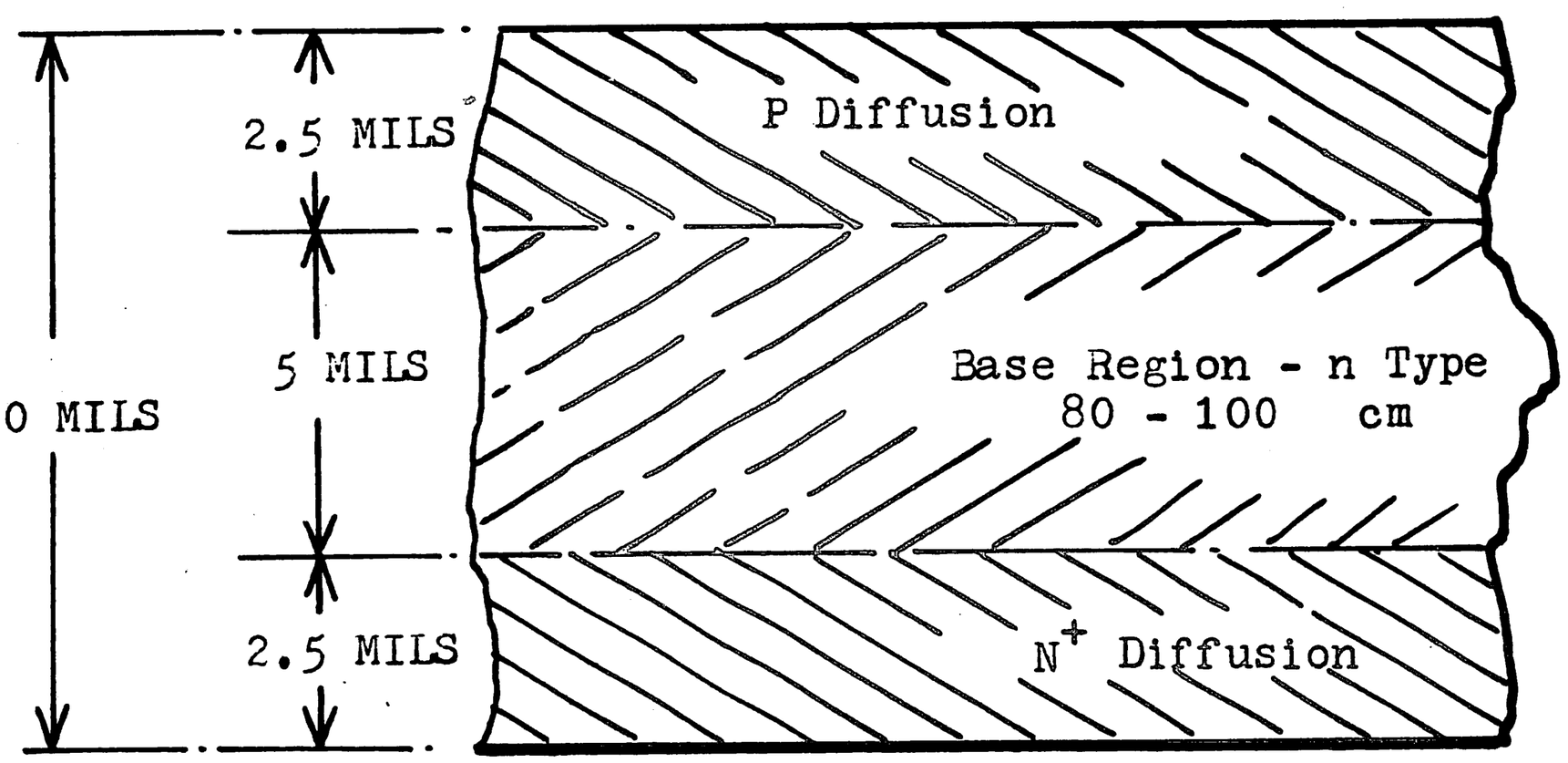
The purpose of this experimental work is to verify equations #43 and #46, and thus to show that $\frac{dC}{dV}$ is related to the second harmonic voltage as predicted by the theory.

The first step is to select a typical silicon planar P-N junction diode with known impurity profile, area, breakdown voltage, and etc. Discussions with Mr. Tom Whalen from the Westinghouse Components Division in Youngwood, Pa. suggested using a 1N4822 diode (see figure 15). This power diode has a large junction area and therefore a larger junction capacitance making measurements practical at lower frequencies. Its breakdown voltage is high, its reverse leakage current small, and the impurity profile is interesting enough to provide an adequate test of the theory.

Next, the $\frac{dC}{dV}$ versus V curve is measured using the standard and straight forward method mentioned in the introduction (p. 15). A one megahertz capacitance bridge is used to measure the variation of capacitance and parallel resistance as functions of voltage. Special care must be taken to insure that the amplitude of the test signal impressed across the diode is always small compared to the D-C bias voltage. In this case an oscilloscope is used to measure and adjust the test

FIGURE 15

PLANAR P-N SILICON DIODE



Type 1N4822

V_b = 1,200 - 1,600 volts

Chip Size = 65 Mils Diameter

Effective Junction Diameter = 55 Mils

Surface Concentration = 10^{21} - 10^{22}/ cm^3

Source of data - Tom Whalen, Youngwood, Pa.

Manufacturer - Westinghouse Electric Corporation

signal of the bridge. The test signal is held constant at 100 millivolts peak to peak to permit capacitance measurement at bias voltages as low as zero volts. The sensitivity of the bridge is reduced somewhat by this low level operation, but is adequate for measurements to within $\pm$.1% (see figure 16 for data).

Capacitance is then plotted versus bias voltage (see figure 17). The derivative is taken point by point to obtain a plot of $\frac{dC}{dV}$ versus V (see figure 18).

Figure 19 shows, in block diagram form, the circuit developed to measure $\frac{dC}{dV}$ versus V directly using harmonic analysis. Development of the actual hardware required to realize this circuit proves to be a rather tricky problem. The first setup using short aligator clip leads spread out on a table proved unsatisfactory due to radiation losses, high series inductance of leads, noise due to insufficient shielding and a poor ground.

A great improvement in performance is achieved by using miniature components and building the entire circuit inside of two Type N connectors. The two female connectors are connected back to back and the two outside bodies grounded and wired together to shield the interior components from noise. This thick shielding wire also provides mechanical support for the device. All leads are clipped short to keep the maximum wire

FIGURE 16

DEPLETION LAYER CAPACITANCE TABLE

BIAS VOLT / VOLT	V_1 out / MV	V_2 out / MV	AMPL CORR / MV	CAPACITANCE BRIDGE PF	CAPACITANCE HARM ANAL PF	CAPACITANCE/VOLT BRIDGE PF/V	CAPACITANCE/VOLT HARM ANAL PF/V	CAPACITANCE/VOLT CORR HARM ANAL PF/V
.5	92	9.2		22.43	19.3			
1.0	86	6.3		19.07	18.0	7		
1.5	74	4.1		16.94	15.5	4		
2.5	62	2.8	.14	14.45	13.0	1.6	1.40	1.33
3.5	58	2.4	.15	14.05	12.2	1.25	1.18	1.06
5	51	1.95	.17	11.52	10.7	.93	.93	.85
7	45	1.55	.20	10.00	9.4	.50	.72	.62
10	42	1.15	.25	8.86	8.8	.33	.52	.41
15	34	.84	.32	7.58	7.1	.20	.38	.24
20	34	.71	.37	6.78	7.1	.14	.31	.14
30	31	.66	.38	5.82	6.5	.07	.28	.09
40	26	.55	.38	5.25	5.4	.05	.23	.06

V_g= .5 V amp

R_s= 52 ohms

R_0= 0 ohms

$|Z_{L1}|$ = 81 ohms

$|Z_{L2}|$ = 72 ohms

ω = 6.28×10^7 rad/sec

DEPLETION LAYER CAPACITANCE VS: BIAS VOLTAGE

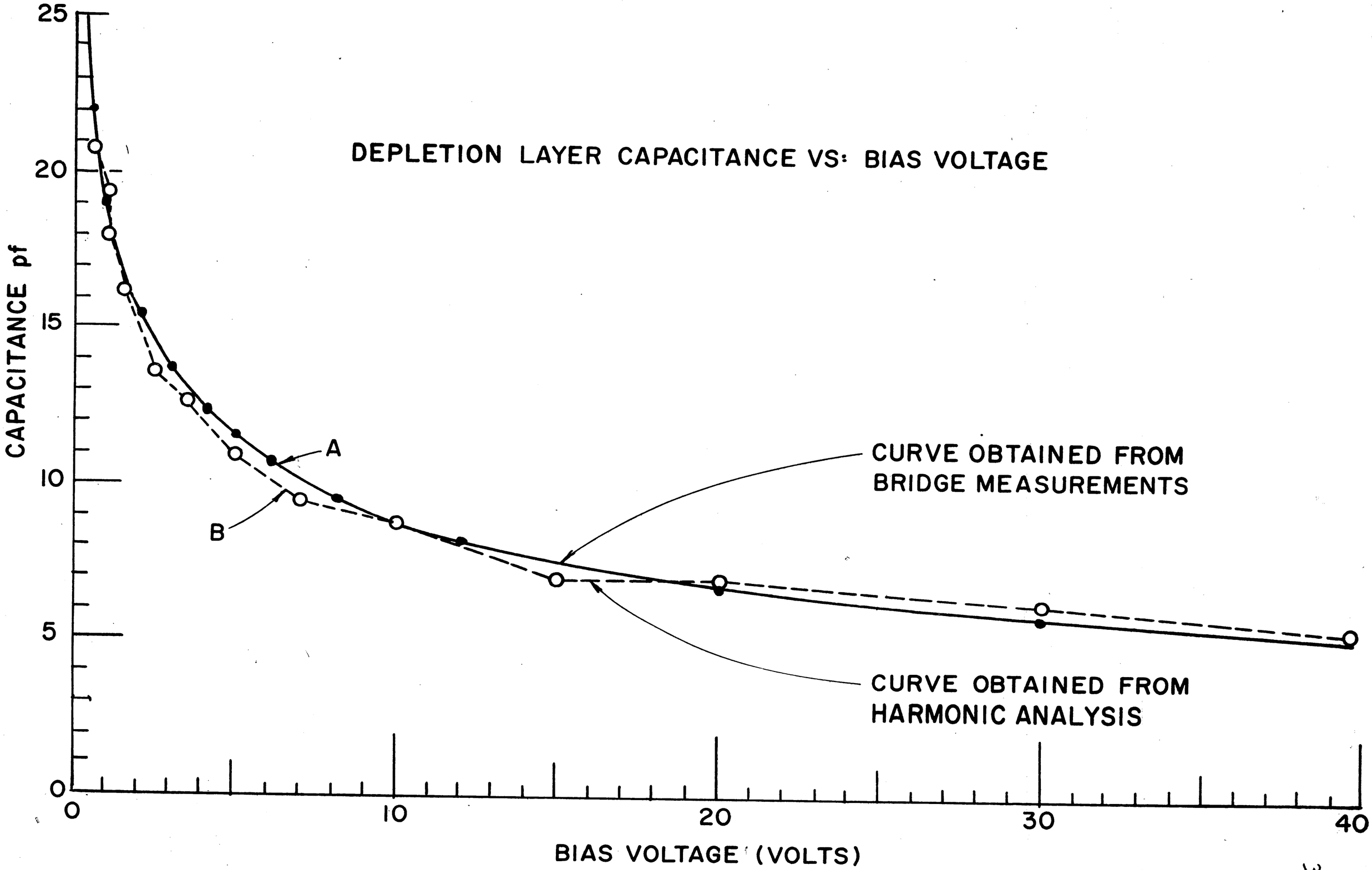


FIGURE 17

FIGURE 18

$\frac{dc}{dv}$ VS: BIAS VOLTAGE

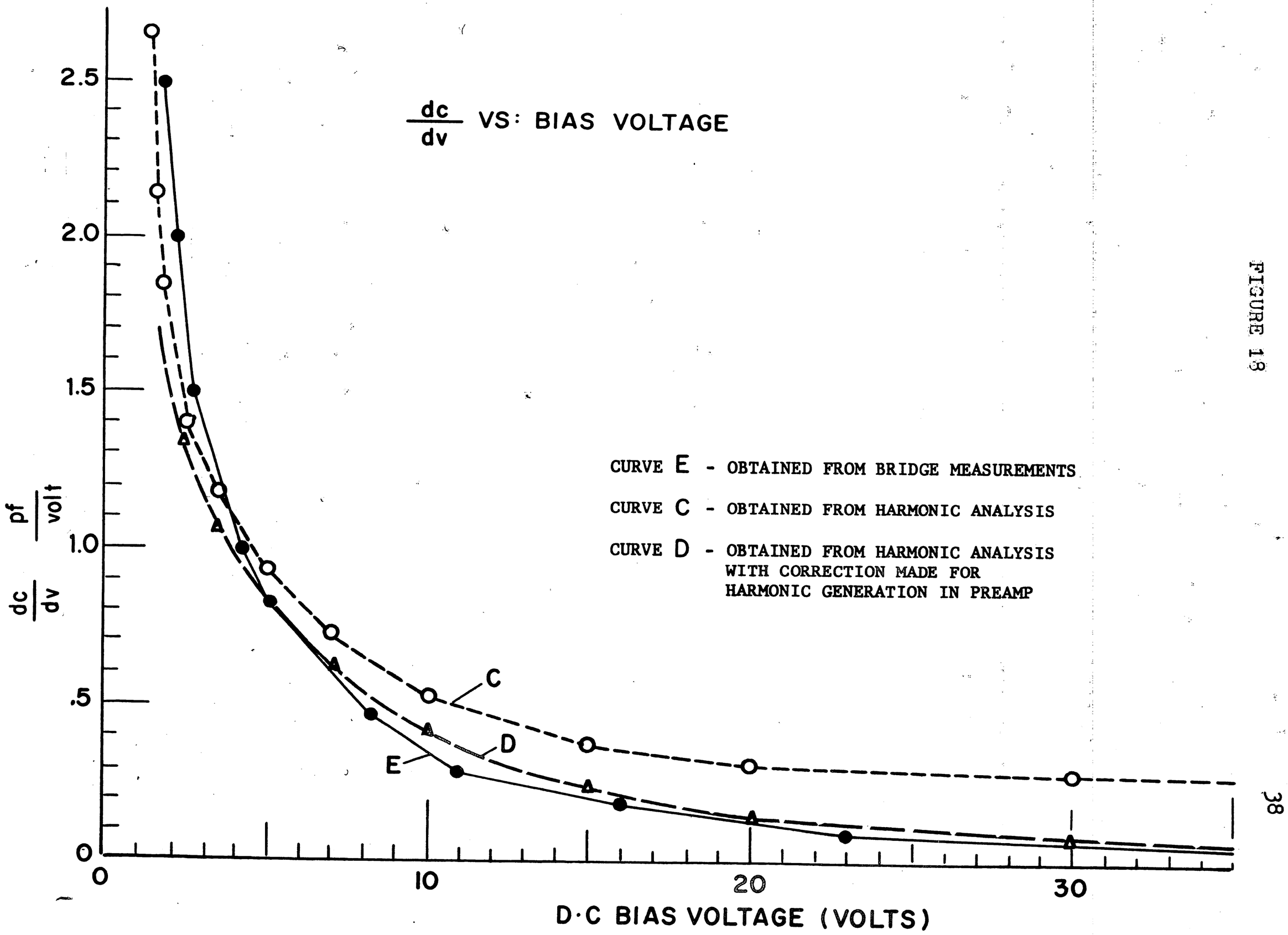
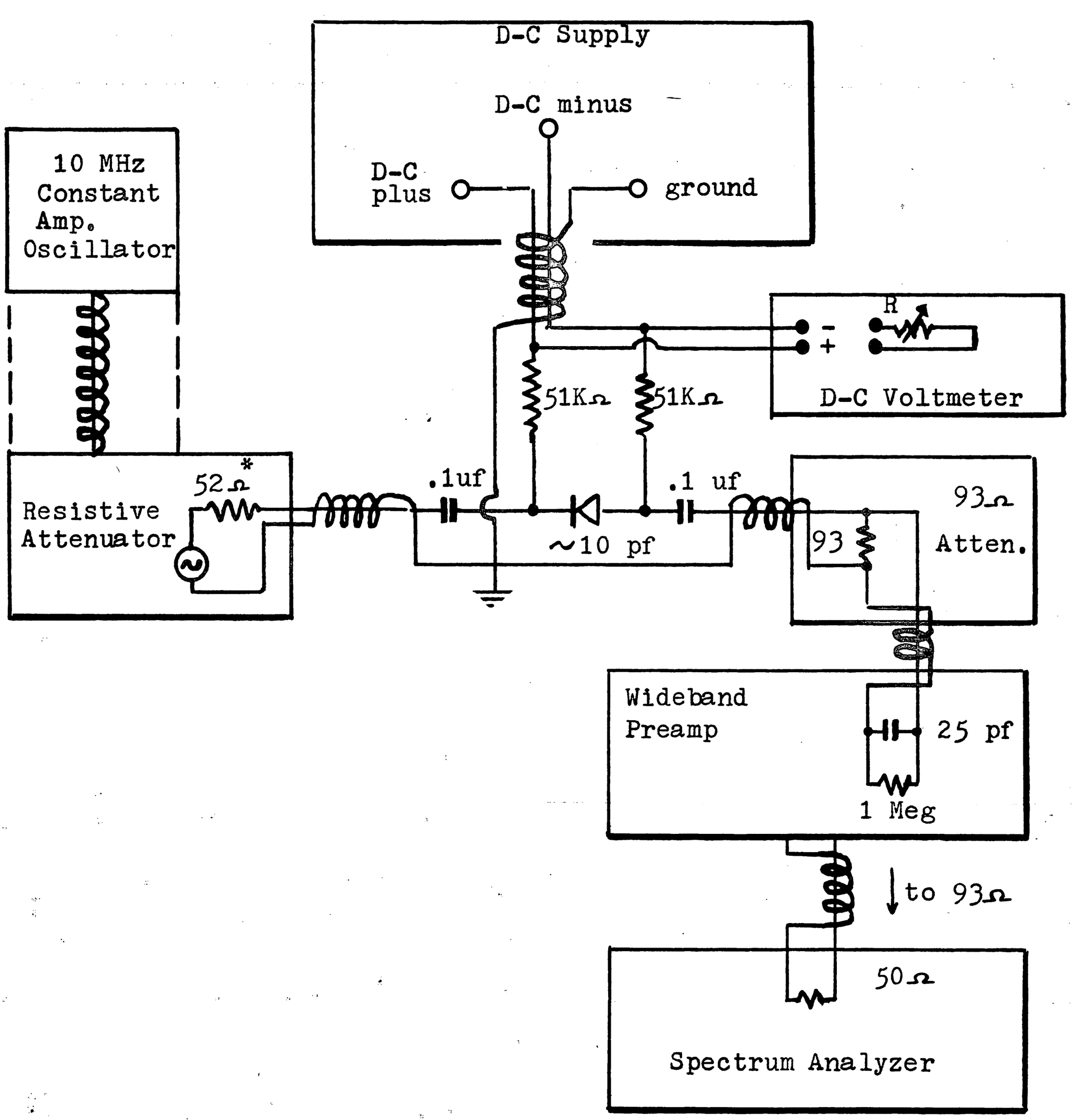


FIGURE 19

CIRCUIT DIAGRAM



* Except when set at 10 volts peak to peak when $R_s = 0\Omega$

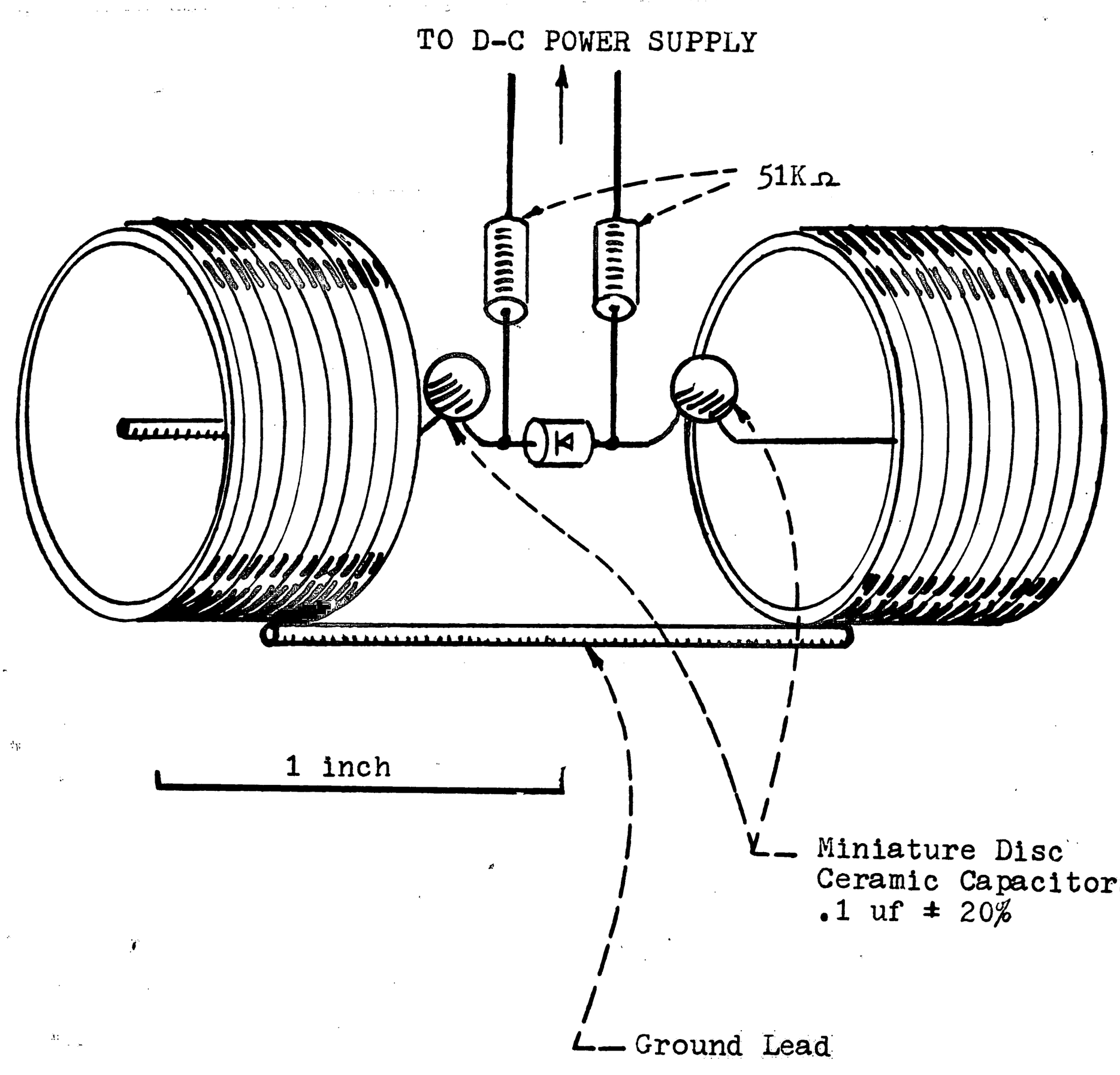
length to less than .5 inches. Ceramic capacitors are used to minimize series inductance. All A-C leads are coaxial cable. A drawing of this connector-circuit arrangement is shown in figure 20.

The A-C signal is supplied by a Tektronix Type 190 Constant Amplitude signal generator set at ten megahertz. This source uses a calibrated attenuator to provide peak to peak output voltages which are continuously variable between four millivolts and ten volts. The impedence looking back into the attenuator is 52 ohms and purely resistive thus providing a matched load for the 50 ohm coaxial line. The attenuator isolates the source from the diode and the matched load prevents power from being reflected back from the signal source.

The D-C bias is provided by a 1.5 amp, 0 - 50 volt, regulated power supply. The leads from this supply are shielded to minimize noise. The small D-C current required to reverse bias the diode feeds through two 51 kilo-ohm isolating resistors located inside the connectors. These resistors are large compared to any A-C impedences in the circuit thus blocking any significant A-C power leakage through them. However, these resistors are small compared to the D-C impedence of the reverse biased diode and so do not significantly affect the biasing voltage.

FIGURE 20

EXPERIMENTAL CIRCUIT



Whereas the two 51 kilo-ohm resistors block A-C currents out of the D-C circuitry without interfering with the D-C currents, the two .1 microfarad ceramic capacitors block the D-C currents from the A-C circuitry without interfering with A-C current flow. These capacitors are an open circuit for D-C but offer an impedence of only 0.16 ohms at ten megahertz.

A Tektronix Wideband Preamp Type 121 with an adjustable voltage gain between .01 and 100 is necessary to provide high enough voltages for accurate measurement in the spectrum analyzer. The spectrum analyzer itself is a Polarad Model STU-1 with an adequate frequency range but a sensitivity of only about 500 millivolts per division. The preamplifier increases the sensitivity to about 5 millivolts per division.

The preamplifier is designed to operate with a 93 ohm line and 93 ohm matched terminations as shown in the circuit diagram. This 93 ohm parallel load reduces the output voltage by a factor of about ten but stops power reflection and improves the linear response of the preamplifier.

The voltage into the spectrum analyzer at any frequency is measured as the height of a spike as displayed on an amplitude versus frequency plot on the

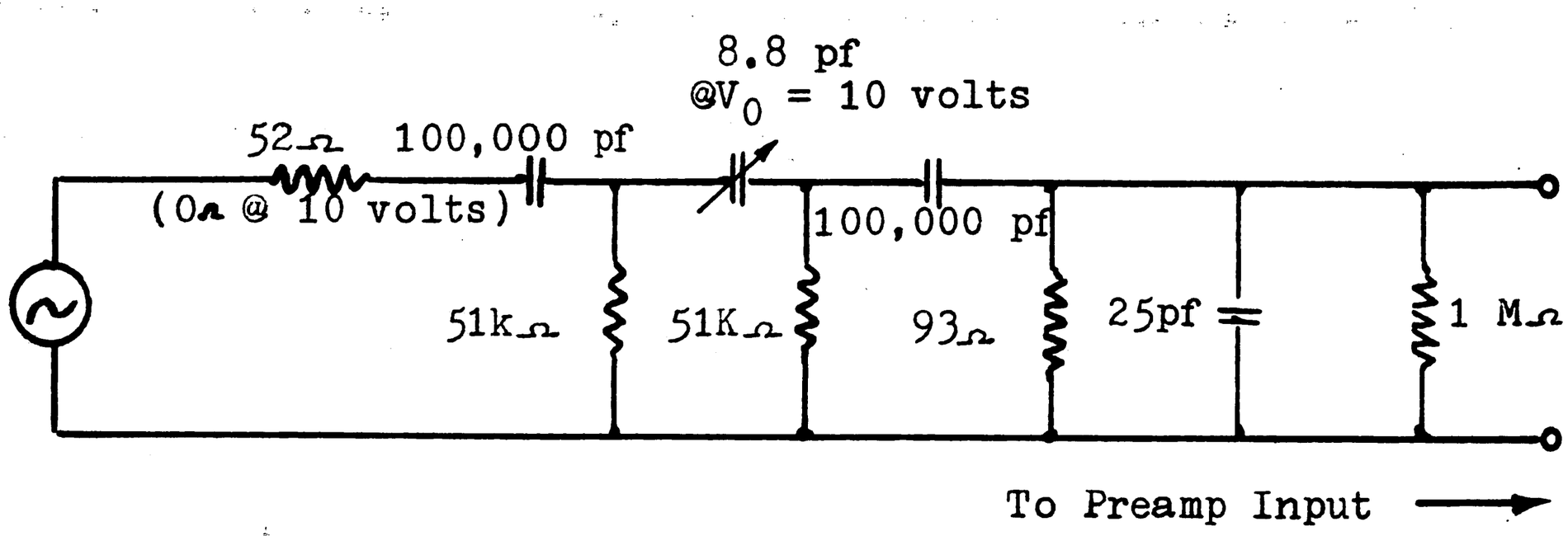
cathode ray tube. Attempts to measure the output voltage directly in this manner are slow and inaccurate due to the rather poor linearity of the spectrum analyzer.

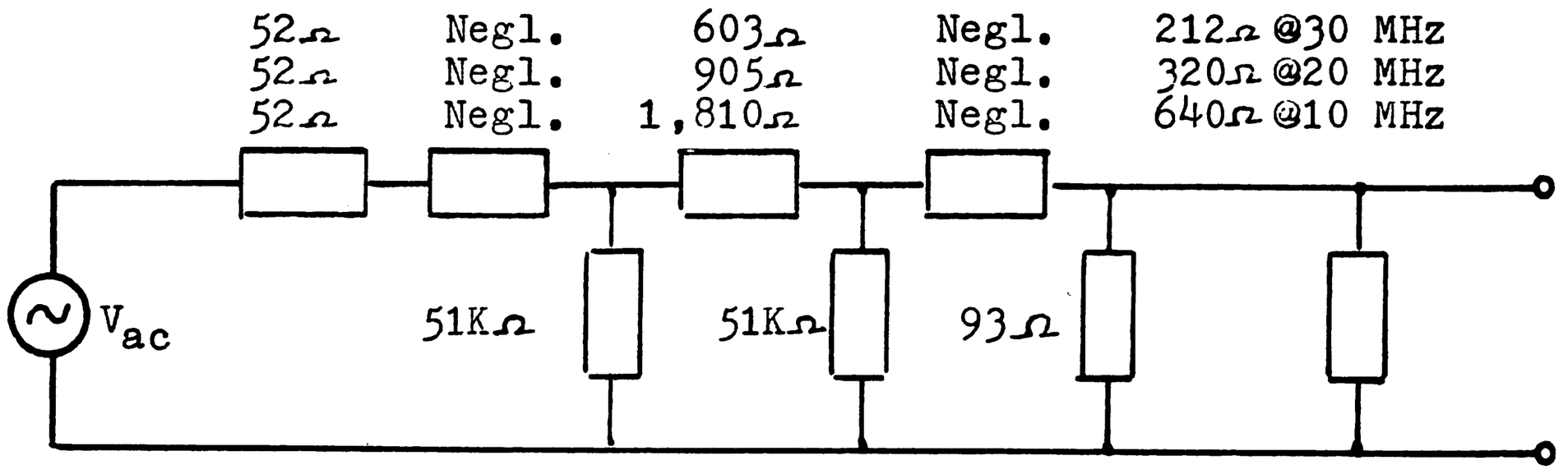
A faster and more accurate method utilizes the gain control of the preamplifier. The constant amplitude signal source and its attenuator are selected as the most accurate and linear elements in the circuit. Using this, known voltages are applied at 10 megahertz, 20 megahertz, and 30 megahertz. The voltages appearing at the input to the attenuator are then calculated from equivalent circuit diagrams (see figure 21). The bridge measured value of C_0 is used at V_0 = 10 volts. This voltage is then compared with the gain setting on the preamplifier required to hold the height of the amplitude spike at that frequency on the harmonic analyzer to an arbitrary but fixed value. From this a purely empirical plot of gain setting versus voltage at the input of the preamplifier can be made. A comparison shows that the voltage at the preamplifier input (see figures 19 and 21) is the same as the V_{out} shown in figure 14.

These plots of gain setting versus input voltage indicate the linearity of the preamplifier. At ten megahertz the linearity of the preamplifier is very good. At higher frequencies the linearity is degraded somewhat and discontinuities develop between scale

FIGURE 21

A-C TEST CIRCUIT MODEL





ranges. These irregularities are compensated for by using these calibration plots in reducing the data.

Using the circuit of figure 21, the voltage outputs (V_{out}) at the fundamental, second harmonic, and third harmonic frequencies are measured for various combinations of input voltage (V_g) and bias voltage (V_0). The calibration curves for the preamplifier are then used to convert gain setting values directly into values of V_{out}.

Some of this reduced data is tabulated in figure 16. The output voltages, V_{out}, at 10 megahertz, 20 megahertz, and 30 megahertz were recorded for values of V_g ranging from 10 millivolts to 10 volts peak to peak. This test procedure was repeated for several different values of bias voltage ranging from .5 volts to 42 volts. The upper limit of the bias voltage is determined by the voltage available from the power supply. Bias voltages less than .5 volts, the lower limit, make even a rough satisfaction of the assumptions of equation #21 impossible. In this case the capacitance is changing very rapidly with bias voltage so that the diode is producing significant harmonic generation at the third and higher harmonics even for small input voltages.

From the data in figure 16, C and $\frac{dC}{dV}$ can be

calculated and plotted as functions of bias voltage. The capacitance, C_0, is calculated from equation #46 and V_{out} fundamental. The derivative of the capacitance, $\frac{dC}{dV}\Big|_{V_0}$, is calculated from equation #43 and V_{out} second harmonic. Both C_0 and $\frac{dC}{dV}\Big|_{V_0}$ are then plotted as functions of V_0 along with values of C_0 and $\frac{dC}{dV}\Big|_{V_0}$ calculated by the bridge method (see figures 17 and 18).

Results

Figure 17 shows a comparison of bridge measurements and harmonic analysis measurements. The plot of C versus V, denoted as curve A, was determined with a one megahertz A-C bridge. Curve B was calculated from equation #46 as derived in the theory section. The bridge measurements are very accurate and yield a smooth curve while the values determined from equation #46 are less precise. However, the agreement between the two curves is generally quite good. Thus values of capacitance calculated by harmonic analysis agree quite well with the values measured on the bridge although the uncertainty of the bridge measurements is much less.

Figure 18 shows a comparison of $\frac{dC}{dV}$ versus V calculated by two different methods. Curve E was obtained simply by measuring the slope of curve A and plotting this as a function of voltage. Although time consuming, this provides a reasonably accurate and reliable measure of $\frac{dC}{dV}$ for use in comparison with this new measurement technique. Curve C shows the results obtained from harmonic analysis.

At low bias levels the agreement between curves C and E is good. However, at higher bias levels the values determined by harmonic analysis are consistantly higher than those determined from bridge measurements.

Assuming the bridge measurements to be reliable and correct, the higher values of $\frac{dC}{dV}$ obtained by harmonic analysis indicate the presence of additional power at the second harmonic generated from sources other than the diode. This could result from sources outside the circuit or from nonlinear elements in the circuit itself. The three primary sources considered are noise, harmonic generation in the oscillator, and harmonic generation in the preamplifier.

The visual display and narrow bandwidth of the Polarad spectrum analyzer makes it possible to actually see and measure the background noise present in the signal. In this experiment, the noise voltage is constant, independent of frequency, and never exceeds 1% of the signal, thus eliminating this as a major source of extra second harmonic power.

The specifications on the Tektronix signal generator limit the total harmonic distortion to a maximum of 5%. Therefore, with the generator output fixed at one volt peak to peak, the amplitude of the second harmonic at the generator output is constant at some voltage less than 50 millivolts peak to peak. The voltage present at the input of the preamplifier due to such a constant harmonic voltage can be calculated. The preceeding derivation in the theory section is directly applicable if we substitute in

$w_0' = 2w_0$. In this case the harmonics of w_0' can be neglected. The output at the second harmonic, w_0', will then follow a curve similar to curve B. Here the output voltage is approximately proportional to the capacitance of the diode. Any error resulting from extra harmonics in the input signal can therefore be expected to be greatest at low bias levels and decrease rapidly as the bias level increases. Actually figure 18 shows that the error is noticeable only at high bias levels and is approximately constant over a wide range. Thus, although a worst case assumption of 5% harmonic distortion from the signal source could be used to explain the magnitude of the error, it cannot account for the peculiar variation of the error magnitude over the range of bias voltages tested. Therefore, harmonic generation in the signal source, if significant at all, is certainly not the dominant effect. This is not surprising since the harmonic content from an oscillator is generally largest when operating near its maximum output power and becomes insignificant at lower power levels.

A third source of extra harmonic power is harmonic generation in the preamplifier due to non-linearity. Even a good vacuum tube amplifier exhibits several percent harmonic distortion when the amplitude of the signal approaches the saturation limit of the

amplifier.(32) With smaller voltage excursions the percent harmonic distortions decreases rapidly becoming negligible for signals with less than a 20% peak to peak excursion. It was initially assumed that since the saturation limit for the preamplifier is two volts peak to peak, and the output of the preamp was held constant at a much smaller value, .03 volts, there would not be any significant harmonic generation in the preamplifier. However, the output was held constant at .03 volts only for the signal being measured. When measuring the amplitude of the fundamental frequency this presents no problem. However, a large amount of amplification is required to bring the amplitude of the second harmonic up to the required .03 volts. With a one volt peak to peak input, the amplitude of the fundamental frequency is 10 to 48 timesthat of the second harmonic and is amplified by the same amount yielding peak to peak voltages between .3 volts and 1.44 volts (see figure 22). When the amplitude of the fundamental frequency exceeds .7 volts, harmonic generation in the preamplifier becomes important. The harmonics produced in the preamplifier add to the harmonics being measured from the diode. The net effect of this process is to transform the saturation limit of the amplifier into a limit on the maximum value of the gain. Placing

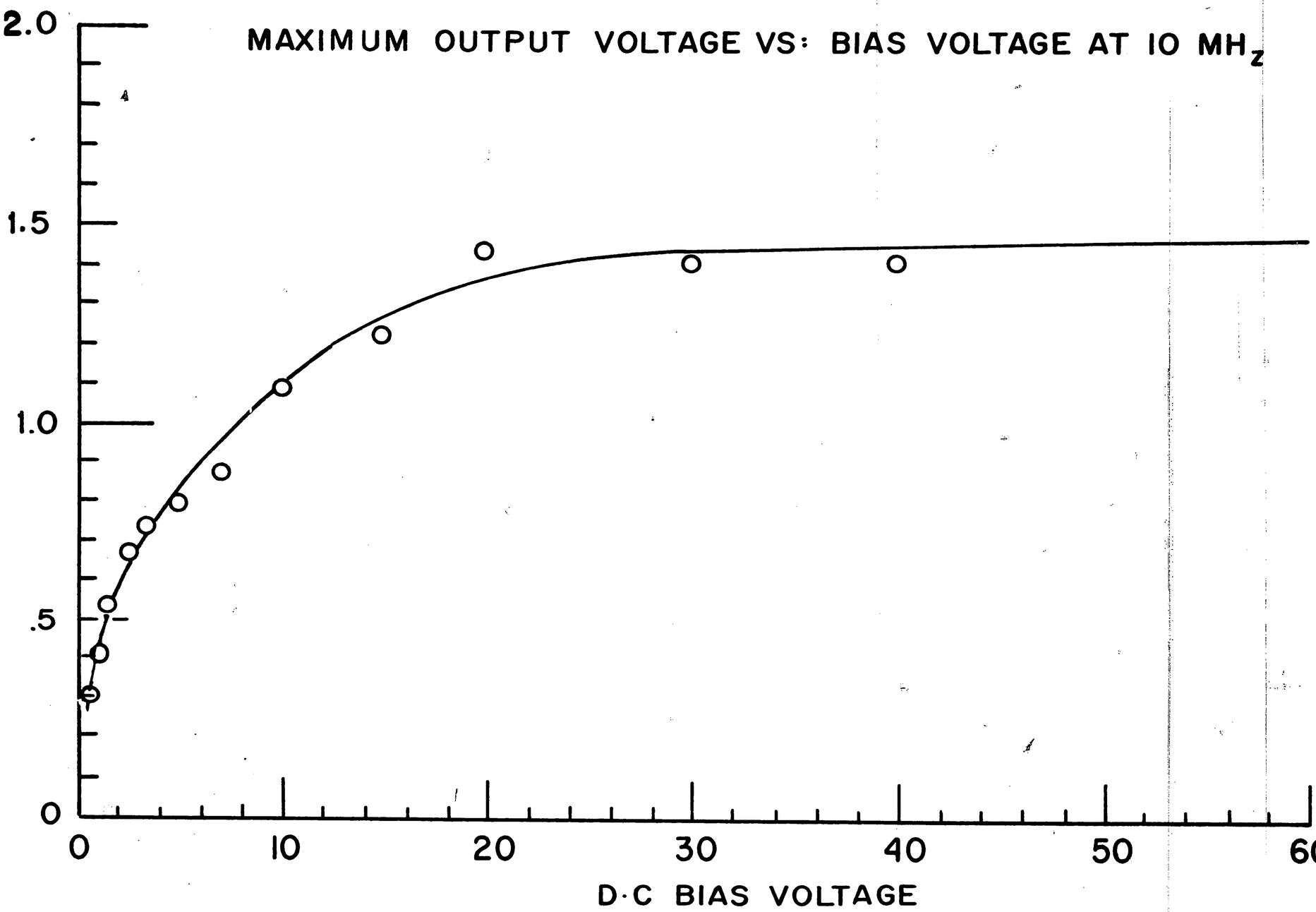

MAXIMUM OUTPUT VOLTAGE VS: BIAS VOLTAGE AT 10 MHz
2.0
1.5
1.0
.5
0
0
10
20
30
40
50
60
D·C BIAS VOLTAGE

FIGURE 22

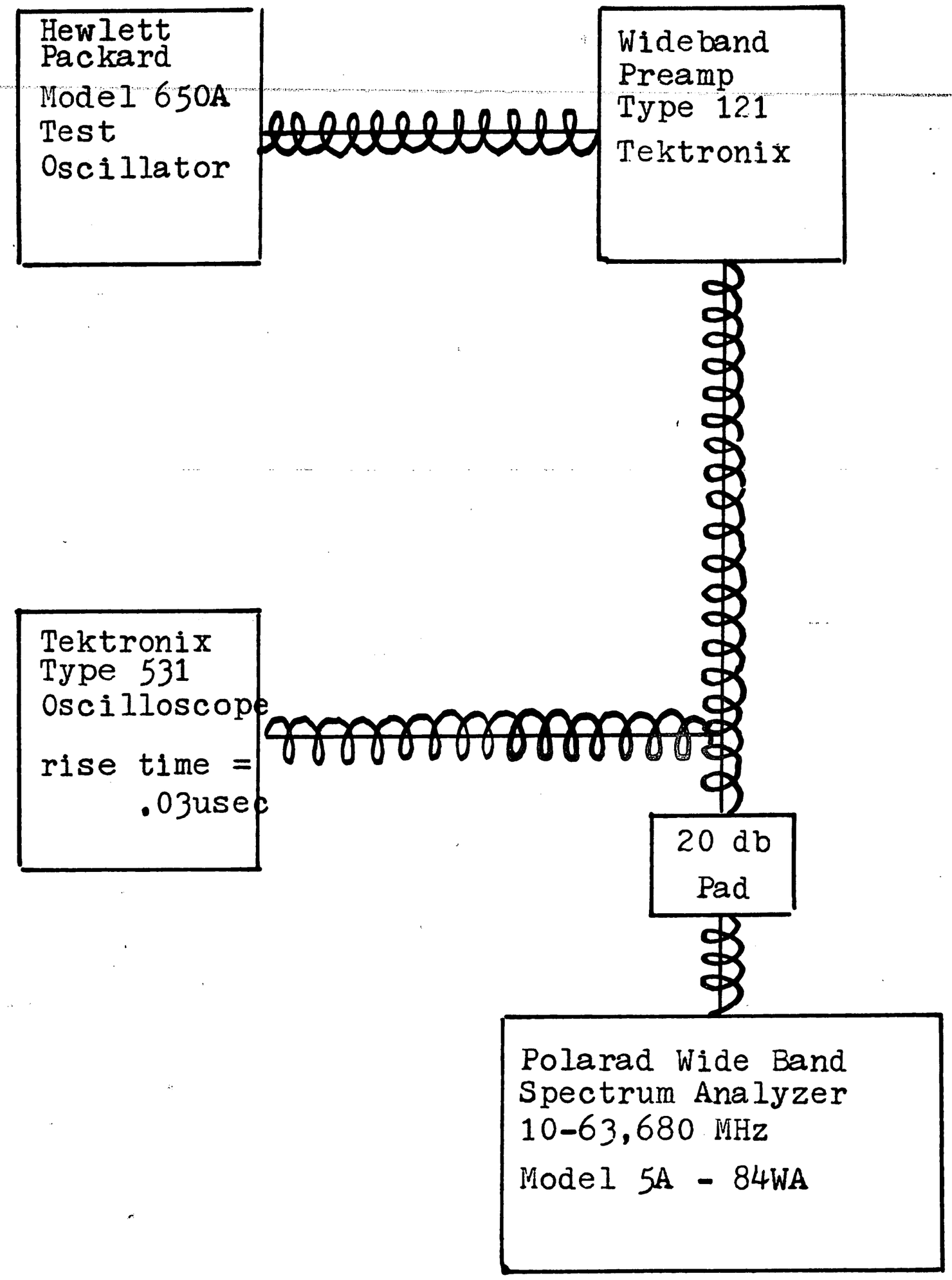
a maximum limit on the gain in turn imposes a minimum limit on the amount of second harmonic measured. This yields a minimum value for the values of $\frac{dC}{dV}$ calculated from equation #43.

To check this theory, an experimental rig was set up to measure harmonic generation in the preamplifier as a function of output voltage (figure 23). The source is set to twenty millivolts peak to peak at ten megahertz. There is no detectable harmonic power in the output of the source. A twenty db attenuation pad is used between the output of the preamp and the spectrum analyzer to prevent overloading of the spectrum analyzer.

The output at both the fundamental frequency and the second harmonic frequency is measured as a function of the output voltage of the preamp (figure 24). The attenuation between the fundamental and the second harmonic is then plotted versus the output voltage. Knowing this relation between the two output voltages enables the calculation of the amplitude of the second harmonic for several values of D-C bias voltage from figure 22 (see figure 25). Returning to the original diode data, one then subtracts from the total observed power that part measured as generated in the preamp. The difference is due to harmonic generation in the diode. This

FIGURE 23

PREAMPLIFIER TEST CIRCUIT



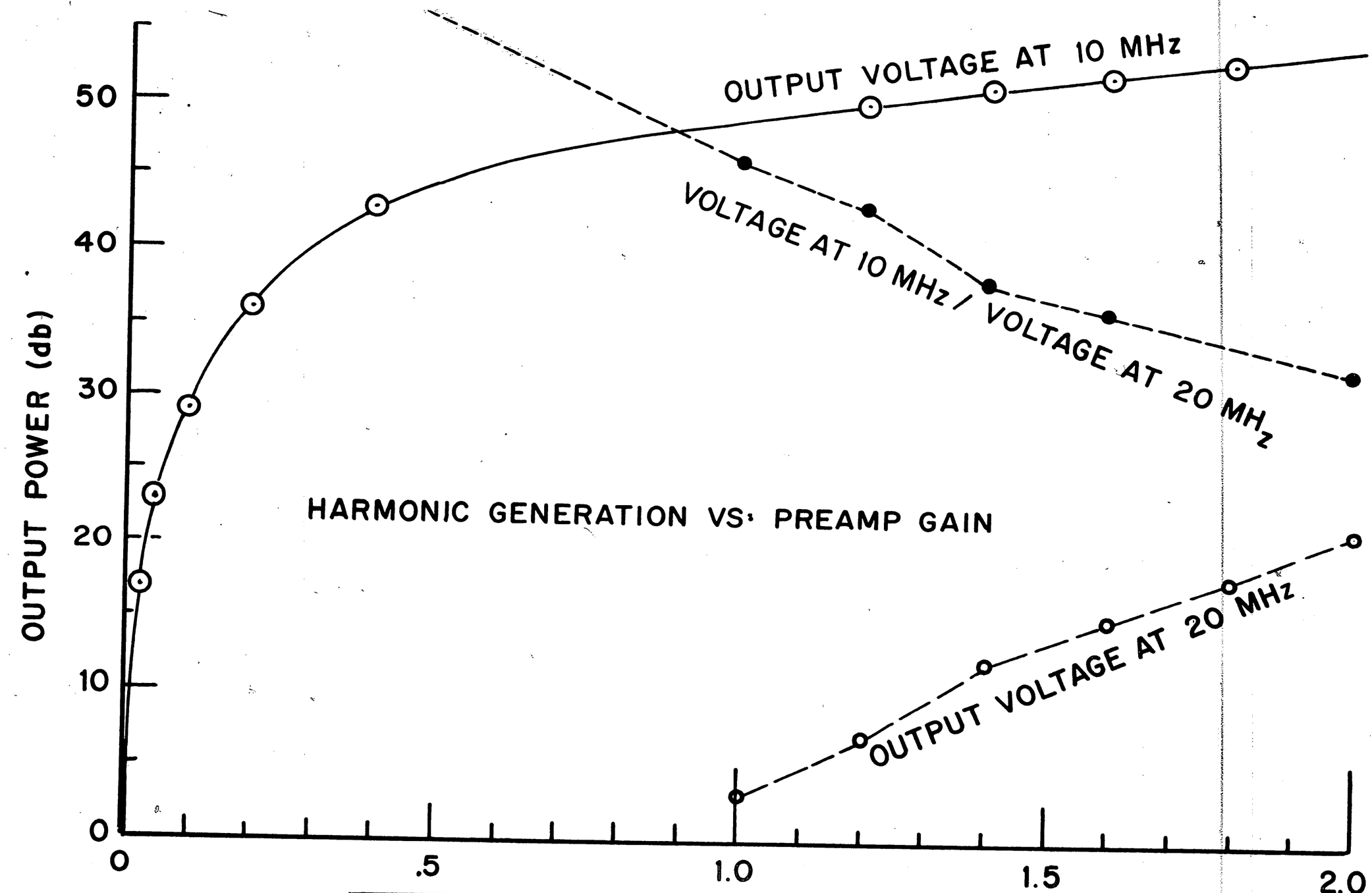

OUTPUT VOLTAGE AT 10 MHz
VOLTAGE AT 10 MHz / VOLTAGE AT 20 MHz
HARMONIC GENERATION VS. PREAMP GAIN
OUTPUT VOLTAGE AT 20 MHz
OUTPUT POWER (db)
50
40
30
20
10
0
0
.5
1.0
1.5
2.0
OUTPUT VOLTAGE (VOLTS)
INPUT = .02 VOLTS PK TO PK
ATTENUATOR PAD = 20 db

FIGURE 24

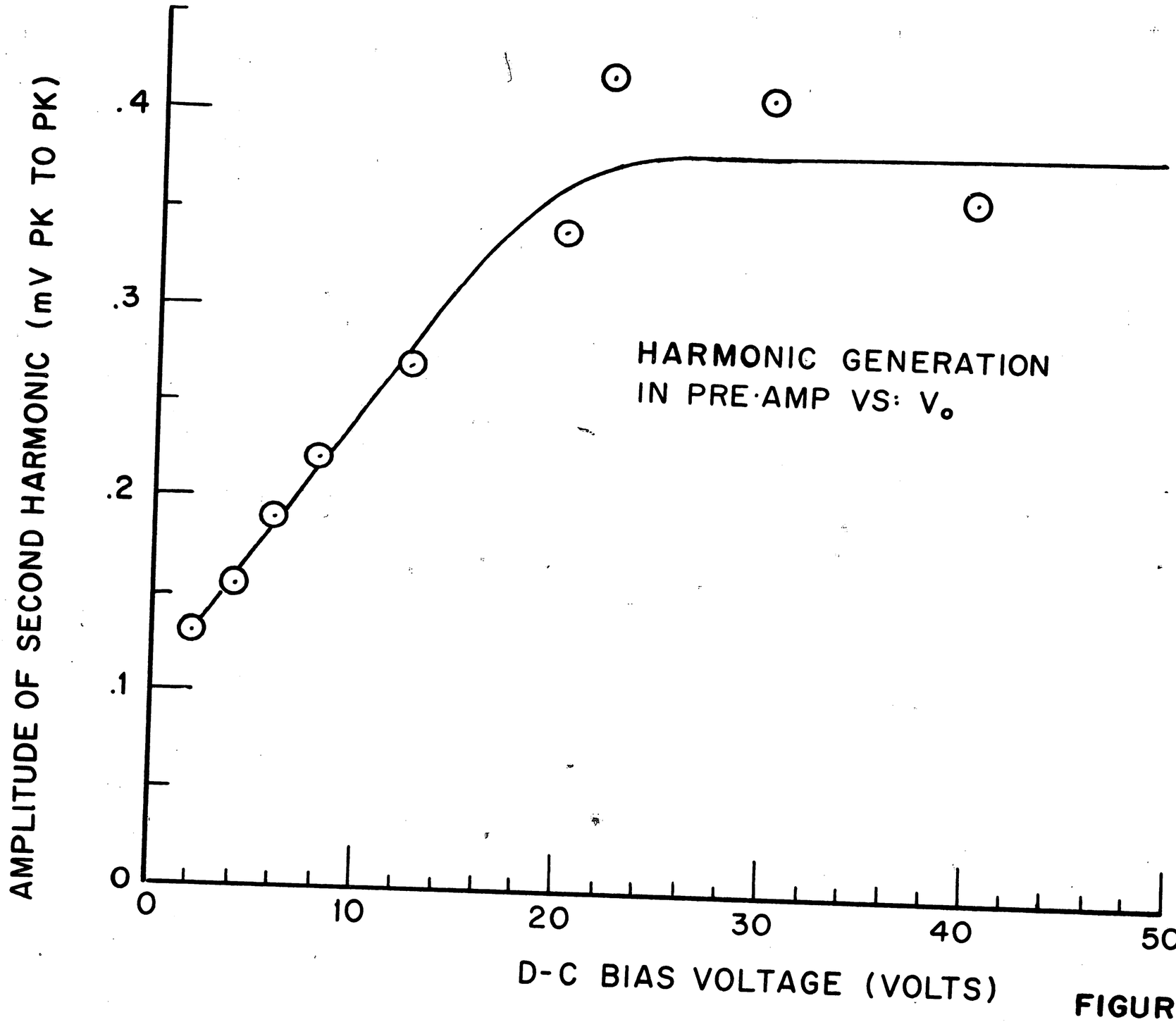

HARMONIC GENERATION
IN PRE-AMP VS: V_o
AMPLITUDE OF SECOND HARMONIC (mV PK TO PK)
.4
.3
.2
.1
0
0
10
20
30
40
50
D-C BIAS VOLTAGE (VOLTS)

FIGURE 25

corrected data is used in equation #43 to obtain a more accurate estimate of $\frac{dC}{dV}$ as a function of bias voltage (see curve D of figure 18). As expected, these values agree much more closely with those obtained with the bridge measurements.

Having measured $\frac{dC}{dV}$ and C as functions of bias, it is now possible to calculate the impurity profile of the diode. In this case N_D and N_A are about the same order of magnitude, thus requiring the use of equation #10 to obtain a more general form of equation #12.

$$(\#52) \quad N_t = \frac{1}{\frac{1}{N_A} + \frac{1}{N_D}} = \frac{C_0^3}{q\epsilon A^2 \frac{dC}{dV}}$$

N_t if first calculated as a function of bias voltage using data from curve E and equation #52. W is calculated as a function of bias voltage using data from curve A and equation #4. N_t is then plotted as a function of W in figure 26 . N_t shows a linear increase with W indicating a linear or graded junction. Caution must be used here as there are non-linear junctions which nevertheless show a linear N_t versus W relation over a fairly wide range.

If $N_D \gg N_A$, then $N_t \approx N_A$ and figure 26 accurately describes the impurity profile on the P side of the junction. If $N_D \ll N_A$, then $N_t \approx N_D$ and figure 26 accurately describes the impurity profile on the N

N_t AS A FUNCTION OF DEPLETION LAYER WIDTH

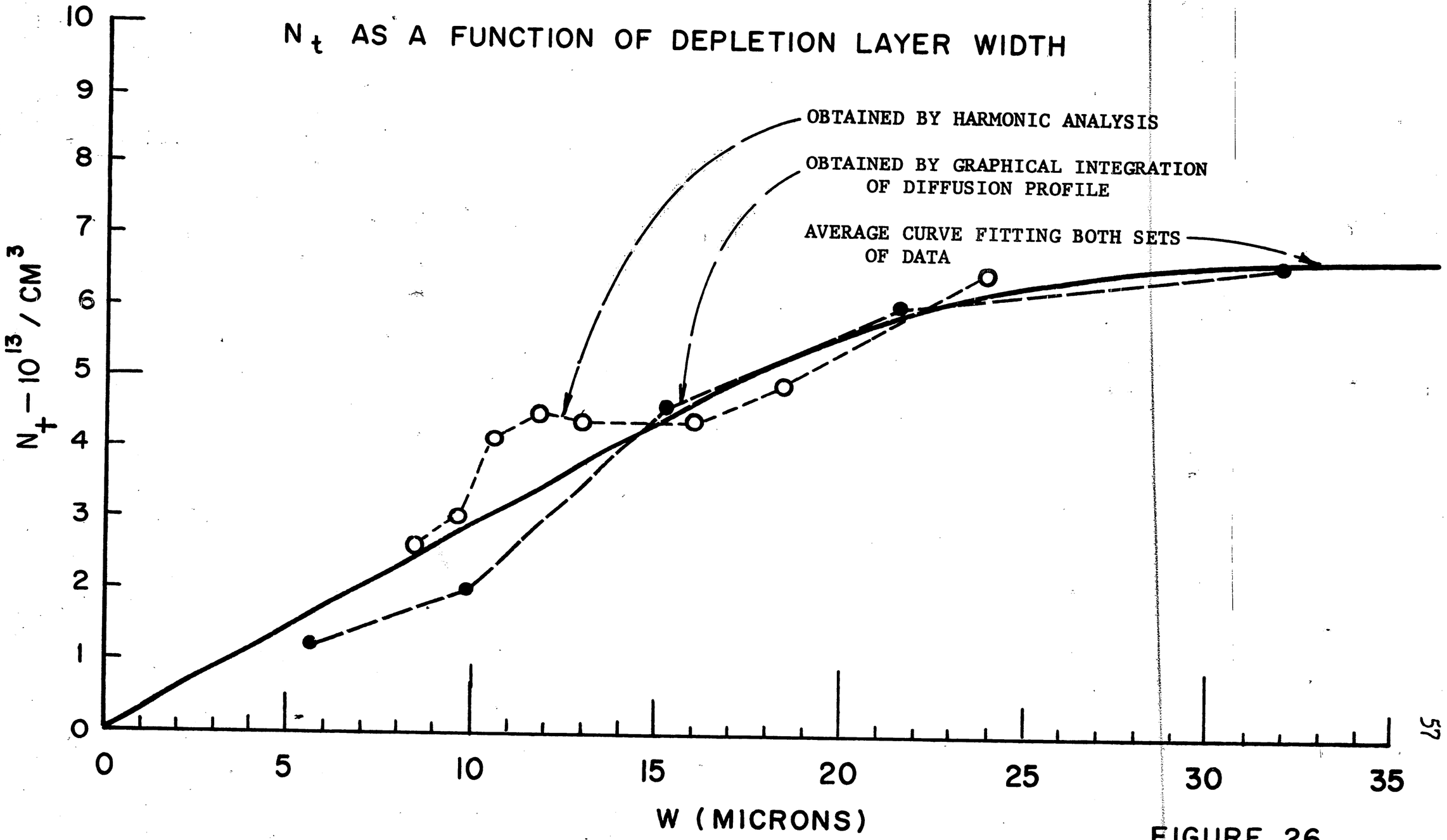


FIGURE 26

side of the junction. However, since $N_A \approx N_D$ then $N_D > N_t < N_A$ and no unique determination of either N_A or N_D is normally possible.

However, the impurity profile of this diode can be calculated from the fabrication data provided by Westinghouse (see figure 27). Using an exponential approximation for describing the impurity distribution near the tail of the P diffusion, the actual impurity profile can be plotted near the junction (see figure 28). Using equal areas to represent equal charge accumulation, N_A and N_D are determined graphically for various values of the depletion layer width, W. N_t is then calculated and plotted on figure 26 along with the data calculated from the capacitance data. Agreement is so good that a single smooth curve can be used to describe both sets of data.

The problem of relating N_t to either N_A or N_D encountered in this example is not typical. In a typical example, where aluminum is used to form the P side of the junction, $N_A \gg N_D$ implies $N_t \approx N_D$.

FIGURE 27 IMPURITY PROFILE OF TEST DIODE

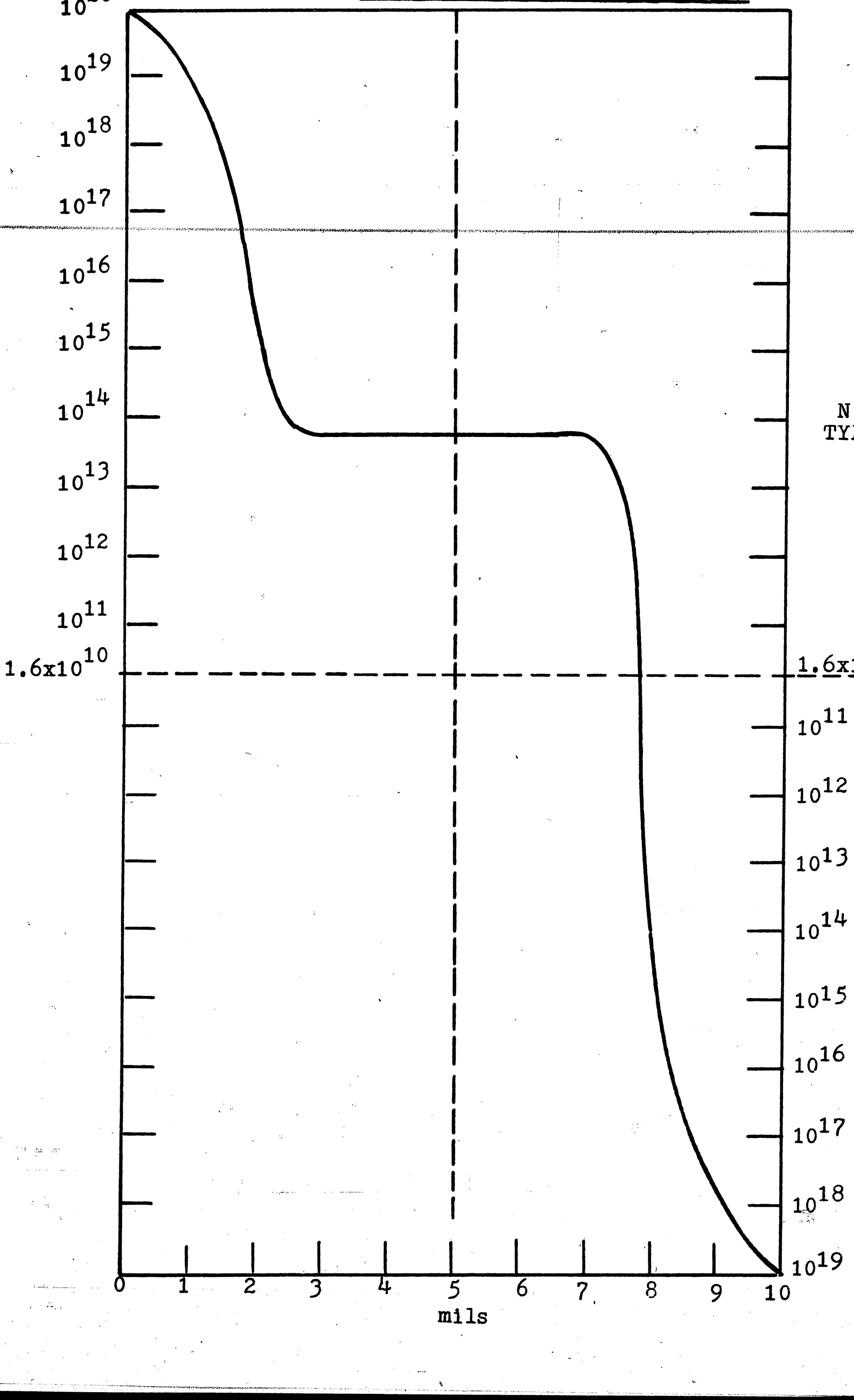
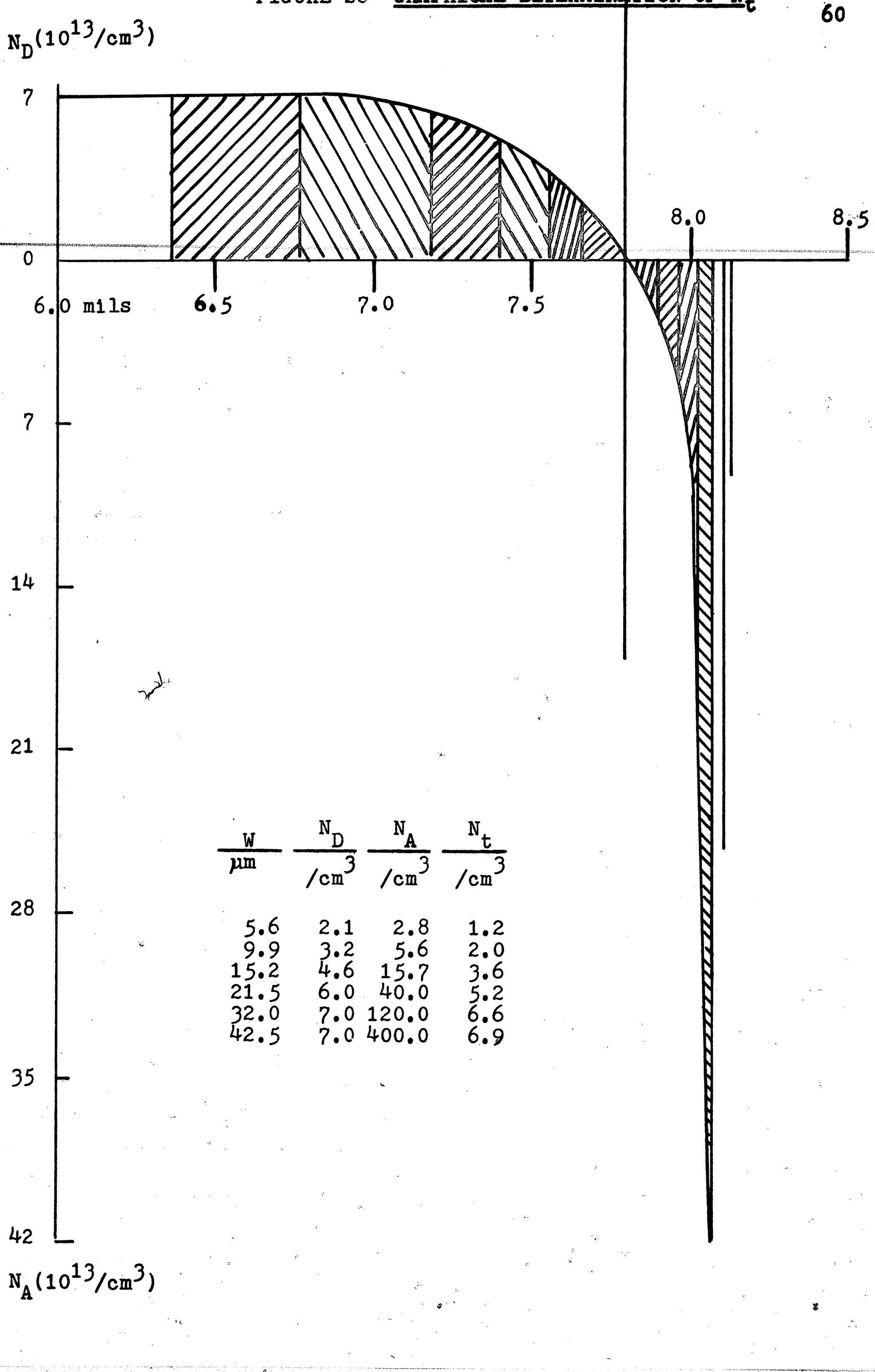


FIGURE 28 GRAPHICAL DETERMINATION OF N_t



W μm	N_D /cm^3	N_A /cm^3	N_t /cm^3
5.6	2.1	2.8	1.2
9.9	3.2	5.6	2.0
15.2	4.6	15.7	3.6
21.5	6.0	40.0	5.2
32.0	7.0	120.0	6.6
42.5	7.0	400.0	6.9

Conclusions

In this paper several different methods for measuring impurity profiles are discussed and compared and a new method presented. The theory for this method is derived and later verified through high frequency experiments. From these experiments the impurity profile of the diode junction is calculated. The results of the harmonic analysis are generally less accurate than those obtained by direct measurements of the capacitance versus voltage relation.

Given a moderate amount of time and money a more sophistocated measurement system could be designed and built. This could provide filtering and separate measurement of both the fundamental and second harmonic frequencies. Several error sources like stray capacitance and inductance, noise, and radiation could be further reduced. However, the greatest problem - unwanted harmonic generation - requires almost perfect linearity in every circuit element. Slight non-linearities in lines, loads, amplifiers, and even the series resistance of the diode itself are expected to continue as the major source of error. Considering this effect, the accuracy of this new method would not be expected to exceed the rather high accuracy possible with

bridge measurements.

The greatest potential advantage of harmonic analysis lies in speed. With separate and simultaneous measurement of both the fundamental and second harmonic frequencies, the bias voltage could be swept with a ramp signal and N_t versus W displayed directly on the X and Y coordinates of an oscilloscope.

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Vita

Roger Green Stewart was born 30 September 1943 in Cheverly, Maryland to Roger D. and Julia G. Stewart. He was raised in the suburbs of Washington, D.C., attending Cheverly Tuxedo Elementary, and Bladensburg Junior High Schools. In June of 1961 he graduated with Honors from Bladensburg High School. The following September he enrolled at the Johns Hopkins University where he received a Bachelor of Engineering Science Degree in Electrical Engineering in June 1965. In September 1965 he enrolled in a Masters Program at Lehigh University.

Mr. Stewart is a member of Eta Kappa Nu and the Institute of Electrical and Electronics Engineers. As an undergraduate he held a Maryland State Defense Scholarship. During graduate study at Lehigh he received aid from the Lehigh Scholarship Fund. During the current year he has filed patent disclosures relating to thin film resistors and light emitting diode arrays. He has had a paper accepted for presentation at the G-MTT Conference in May 1968 on X Band Diode Phase Shifters.

Professionally, Mr. Stewart worked for the Goddard Space Flight Center in Greenbelt, Maryland as an engineering assistant between sessions at Johns Hopkins University. During the summer of 1963 he was invited to join with the University as a student

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